PROBABLE QUESTION & ANSWER

SUBJECT-MPMC *SEMESTER-6TH* *BRANCH-EE & EEE*

1. Which of the following is correct for microprocessor Intel 8085?
a) 8 bit microprocessor
b) 16 bit microprocessor
c) 4 bit microprocessor
d) 32 bit microprocessor
View Answer
Answer: a
Explanation: Microprocessor Intel 8085 is an 8 bit microprocessor.

2. MOS stands for _____
a) Material Operating Semiconductor
b) Metal Oxide Semiconductor
c) Metal Operating Segment
d) None of the mentioned
View Answer
Answer: b
Explanation: MOS or Metal Oxide Semiconductor is an IC technology.

3. Microprocessor contains large on-chip memory.
a) True
b) False
View Answer
Answer: b
Explanation: Microprocessor is a small version of the processor which lack on-chip memory.

4. Which of the following part of the microprocessor is close related to register?
a) Processor
b) CPU
c) ALU
d) Memory
View Answer
Answer: d
Explanation: Registers are basically memory segments used for storing the address of locations.

5. Which of the following is not a special function register?
a) Program counter
b) Instruction pointer
c) Accumulator
d) Stack pointer
View Answer

Answer: c
Explanation: Accumulator is a general function register, which can be used for multiple functions.

6. SP stands for _____
a) Stack pointer
b) Segment pointer
c) Status pointer
d) State pointer
View Answer
Answer: a
Explanation: SP is the short form of stack pointer which store address of stack top.

7. Which of the following is not a valid instruction type?
a) Zero operant
b) Single operand
c) Two operand
d) None of the mentioned
View Answer
Answer: d
Explanation: Instructions are divided into different types according to the number of operands.

8. How many flags does 8085 have?
a) 4
b) 5
c) 8
d) 9
View Answer
Answer: c
Explanation: 8085 contains 5 flags such as sign flag, zero flag, parity flag, auxiliary carry flag, and carry flag.

9. Which of the following is used for storing flag registers?
a) Status register
b) Control register
c) Buffer register
d) None of the mentioned
View Answer
Answer: a
Explanation: Status registers are used for storing flag registers.

10. Which of the following function relate to stack?
a) Push and pop
b) Call and return
c) Both push pop and call return
d) None of the mentioned
View Answer

Answer: a
Explanation: Push function is used for inserting value to stack and pop is used for retrieving data from the stack.

11. 8085 microprocessor is an 8-bit microprocessor designed by?
A. IBM
B. Dell
C. Intel
D. VAX
View Answer
Ans : C
Explanation: 8085 is pronounced as "eighty-eighty-five" microprocessor. It is an 8-bit microprocessor designed by Intel in 1977.

12. In 8085, 16-bit address bus, which can address upto?
A. 16KB
B. 32KB
C. 64KB
D. 128KB
View Answer
Ans : C
Explanation: In 8085, 16-bit address bus, which can address upto 64KB.

13. There are _____ general purpose registers in 8085 processor
A. 5
B. 6
C. 7
D. 8
View Answer
Ans : B
Explanation: There are 6 general purpose registers in 8085 processor, i.e. B, C, D, E, H & L. Each register can hold 8-bit data.

14. It is also a 16-bit register works like stack, which is always incremented/decremented by 2 during push & pop operations.

A. Stack pointer
B. Temporary register
C. Flag register
D. Program counter
View Answer
Ans : A

Explanation: Stack pointer : It is also a 16-bit register works like stack, which is always incremented/decremented by 2 during push & pop operations.

15. Flag register is an 8-bit register having _____ 1-bit flip-flops.
A. 3
B. 4
C. 5
D. 6
View Answer

Ans : C

Explanation: These are the set of 5 flip-flops : Sign (S), Zero (Z), Auxiliary Carry (AC), Parity (P) and Carry (C)

16. What is true about Program counter?

A. It is an 8-bit register, which holds the temporary data of arithmetic and logical operations.
B. When an instruction is fetched from memory then it is stored in the program counter
C. It provides timing and control signal to the microprocessor
D. It is a 16-bit register used to store the memory address location of the next instruction to be executed.

View Answer
Ans : D
Explanation: Program counter : It is a 16-bit register used to store the memory address location of the next instruction to be executed.

17. This signal indicates that another master is requesting the use of the address and data buses.

A. READY
B. HOLD
C. HLDA
D. INTA
View Answer
Ans : B
Explanation: HOLD : This signal indicates that another master is requesting the use of the address and data buses.

18. This signal is used as the system clock for devices connected with the microprocessor.

A. X1, X2
B. CLK OUT
C. CLK IN
D. IO/M

View Answer
Ans : B
Explanation: CLK OUT : This signal is used as the system clock for devices connected with the microprocessor.

19. Which of the following is true about Control and status signals?

A. These signals are used to identify the nature of operation.
B. There are 3 control signal and 3 status signals.
C. Three status signals are IO/M, S0 & S1.
D. All of the above

View Answer
Ans : D

Explanation: All of the above are correct about Control and status signals.

20. MVI K, 20F is an example of?

A. Immediate addressing mode
B. Register addressing mode

C. Direct addressing mode
D. Indirect addressing mode
View Answer
Ans : A
Explanation: Immediate addressing mode : In this mode, the 8/16-bit data is specified in the instruction itself as one of its operand. For example: MVI K, 20F: means 20F is copied into register K

21. Operation code field is present in :
a) programming language instruction
b) assembly language instruction
c) machine language instruction
d) none of the mentioned
View Answer
Answer: c
Explanation: Machine language instruction format has one or more fields. The first one is the operation code field.

22. A machine language instruction format consists of
a) Operand field
b) Operation code field
c) Operation code field & operand field
d) none of the mentioned
View Answer
Answer: c
Explanation: Machine language instruction format has both the fields.

23. The length of the one-byte instruction is
a) 2 bytes
b) 1 byte
c) 3 bytes
d) 4 bytes
View Answer
Answer: b
Explanation: This format is only one byte long.

24. The instruction format ‘register to register’ has a length of
a) 2 bytes
b) 1 byte
c) 3 bytes
d) 4 bytes
View Answer
Answer: a
Explanation: This format is 2 bytes long.

25. The R/M field in a machine instruction format specifies
a) another register
b) another memory location
c) other operands

d) all of the mentioned
View Answer
Answer: d
Explanation: The LSBs(least significant bits) from 0 to 3 represent R/M field that specifies another register or memory location i.e. the other operand.

26. The instruction, MOV AX, 0005H belongs to the address mode
a) register
b) direct
c) immediate
d) register relative
View Answer
Answer: c
Explanation: In Immediate addressing mode, immediate data is a part of instruction and appears in the form of successive byte or bytes.

27. The instruction, MOV AX, 1234H is an example of
a) register addressing mode
b) direct addressing mode
c) immediate addressing mode
d) based indexed addressing mode
View Answer
Answer: c
Explanation: Since immediate data is present in the instruction.

28. The instruction, MOV AX, [2500H] is an example of
a) immediate addressing mode
b) direct addressing mode
c) indirect addressing mode
d) register addressing mode
View Answer
Answer: b
Explanation: Since the address is directly specified in the instruction as a part of it.

29. If the data is present in a register and it is referred using the particular register, then it is
a) direct addressing mode
b) register addressing mode
c) indexed addressing mode
d) immediate addressing mode
View Answer
Answer: b
Explanation: Since register is used to refer the address.

30. The instruction, MOV AX,[BX] is an example of
a) direct addressing mode
b) register addressing mode
c) register relative addressing mode
d) register indirect addressing mode
View Answer

Answer: d
Explanation: Since the register used to refer to the address is accessed indirectly.

31. The instruction that is used to transfer the data from source operand to destination operand is
a) data copy/transfer instruction
b) branch instruction
c) arithmetic/logical instruction
d) string instruction
View Answer
Answer: a
Explanation: These instructions are used to copy and transfer the instructions.

32. Which of the following is not a data copy/transfer instruction?
a) MOV
b) PUSH
c) DAS
d) POP
View Answer
Answer: c
Explanation: DAS (Decimal Adjust after Subtraction) is an arithmetic instruction.

33. The instructions that involve various string manipulation operations are
a) branch instructions
b) flag manipulation instructions
c) shift and rotate instructions
d) string instructions
View Answer
Answer: d
Explanation: The string instructions perform operations on strings such as load, move, scan, compare etc.

34. Which of the following instruction is not valid?
a) MOV AX, BX
b) MOV DS, 5000H
c) MOV AX, 5000H
d) PUSH AX
View Answer
Answer: b
Explanation: Both the source and destination operands cannot be memory locations except for string instructions.

35. In PUSH instruction, after each execution of the instruction, the stack pointer is
a) incremented by 1
b) decremented by 1
c) incremented by 2
d) decremented by 2
View Answer
Answer: d
Explanation: The actual current stack-top is always occupied by the previously pushed data.

So, the push operation decrements SP by 2 and then stores the two bytes contents of the operand onto the stack.

36. The instruction that pushes the contents of the specified register/memory location on to the stack is
a) PUSHF
b) POPF
c) PUSH
d) POP
View Answer
Answer: c
Explanation: Since PUSH operation transfers data to stack from a register or memory location.

37. In POP instruction, after each execution of the instruction, the stack pointer is
a) incremented by 1
b) decremented by 1
c) incremented by 2
d) decremented by 2
View Answer
Answer: c
Explanation: The actual current stack top is poped into the specific operand as the contents of stack top memory is stored in AL&SP and further contents of the memory location pointed to by SP are copied to AH & SP.

38. The instructions that are used for reading an input port and writing an output port respectively are
a) MOV, XCHG
b) MOV, IN
c) IN, MOV
d) IN, OUT
View Answer
Answer: d
Explanation: The address of the input/output port may be specified directly or indirectly.
Example for input port: IN AX, DX; This instruction reads data from a 16-bit port whose address is in DX and stores it in AX
Example for output port: OUT 03H, AL; This sends data available in AL to a port whose address is 03H.

39. The instruction that is used for finding out the codes in case of code conversion problems is
a) XCHG
b) XLAT
c) XOR
d) JCXZ
View Answer
Answer: b
Explanation: The translate(XLAT) instruction is used to find codes.

40. The instruction that loads effective address formed by destination operand into the specified source register is
a) LEA
b) LDS
c) LES
d) LAHF
View Answer
Answer: a
Explanation: The instruction, LEA loads effective address and is more useful for assembly language rather than for machine language.

41. The instruction that loads the AH register with the lower byte of the flag register is
a) SAHF
b) AH
c) LAHF
d) PUSHF
View Answer
Answer: c
Explanation: The instruction LAHF(Load AH from a lower byte of Flag) may be used to observe the status of all the condition code flags(except overflow flag) at a time.

42. The instruction that pushes the flag register on to the stack is
a) PUSH
b) POP
c) PUSHF
d) POPF
View Answer
Answer: c
Explanation: The instruction PUSHF(push flags to stack) pushes the flag register on to the stack.

43. The instruction that loads the flag register completely from the word contents of the memory location is
a) PUSH
b) POP
c) PUSHF
d) POPF
View Answer
Answer: d
Explanation: POPF is pop flags to stack.

44. The instruction that adds immediate data/contents of the memory location specified in an instruction/register to the contents of another register/memory location is
a) SUB
b) ADD
c) MUL
d) DIV
View Answer

Answer: b
Explanation: ADD instruction adds the data.

45. The instruction that supports addition when carry exists is
a) ADD
b) ADC
c) ADD & ADC
d) None of the mentioned
View Answer
Answer: b
Explanation: ADC(Add with Carry) instruction performs the same operation as ADD operation, but adds the carry flag bit to the result.

46. The instruction, “INC” increases the contents of the specified register or memory location by
a) 2
b) 0
c) 1
d) 3
View Answer
Answer: c
Explanation: This instruction adds 1 to the contents of the operand and so increments by 1.

47. The instruction that subtracts 1 from the contents of the specified register/memory location is
a) INC
b) SUBB
c) SUB
d) DEC
View Answer
Answer: d
Explanation: The DEC instruction decrements the contents of a specified register/memory location by 1.

48. The instruction that enables subtraction with borrow is
a) DEC
b) SUB
c) SBB
d) None of the mentioned
View Answer
Answer: c
Explanation: The SBB instruction subtracts the source operand and the borrow flag from the destination operand.

49. The flag that acts as Borrow flag in the instruction, SBB is
a) direction flag
b) carry flag
c) parity flag
d) trap flag
View Answer

Answer: b
Explanation: If borrow exists in the subtraction operation performed then carry flag is set.

50. In general, the source operand of an instruction can be
a) memory location
b) register
c) immediate data
d) all of the mentioned
View Answer
Answer: d
Explanation: The source operand is the element which is data or data stored memory location on which operation is performed.

51. The assembler directives which are the hints using some predefined alphabetical strings are given to
a) processor
b) memory
c) assembler
d) processor & assembler
View Answer
Answer: c
Explanation: These directives help the assembler to correctly understand the assembly language programs to prepare the codes.

52. The directive used to inform the assembler, the names of the logical segments to be assumed for different segments used in the program is
a) ASSUME
b) SEGMENT
c) SHORT
d) DB
View Answer
Answer: a
Explanation: In ALP, each segment is given a name by using the directive ASSUME
SYNTAX: ASSUME segment:segment_name
Eg: ASSUME CS:Code
here CS is the Code segment and code is the name assumed to the segment.

53. Match the following

```
a) DB          1) used to direct the assembler to reserve only 10-bytes
b) DT          2) used to direct the assembler to reserve only 4 words
c) DW          3) used to direct the assembler to reserve byte or bytes
d) DQ          4) used to direct the assembler to reserve words
```

a) a-3, b-2, c-4, d-1
b) a-2, b-3, c-1, d-4
c) a-3, b-1, c-2, d-4
d) a-3, b-1, c-4, d-2
View Answer

Answer: d
Explanation: These directives are used for allocating memory locations in the available memory.

54. The directive that marks the end of an assembly language program is
a) ENDS
b) END
c) ENDS & END
d) None of the mentioned
View Answer
Answer: b
Explanation: The directive END is used to denote the completion of the program.

55. The directive that marks the end of a logical segment is
a) ENDS
b) END
c) ENDS & END
d) None of the mentioned
View Answer
Answer: a
Explanation: The directive ENDS is used to end a segment where as the directive END is used to end the program.

56. The directive that updates the location counter to the next even address while executing a series of instructions is
a) EVN
b) EVEN
c) EVNE
d) EQU
View Answer
Answer: b
Explanation: The directive updates location counter to next even address if the current location counter contents are not even.

57. The directive that directs the assembler to start the memory allotment for a particular segment/block/code from the declared address is
a) OFFSET
b) LABEL
c) ORG
d) GROUP
View Answer
Answer: c
Explanation: If an ORG is written then the assembler initiates the location counter to keep the track of allotted address for the module as mentioned in the directive.
If the directive is not present, then the location counter is initialized to 0000H.

58. The directive that marks the starting of the logical segment is
a) SEG
b) SEGMENT
c) SEG & SEGMENT

d) PROC
View Answer
Answer: b
Explanation: The directive SEGMENT indicates the beginning of the segment.

59. The recurrence of the numerical values or constants in a program code is reduced by
a) ASSUME
b) LOCAL
c) LABEL
d) EQU
View Answer
Answer: d
Explanation: In this, the recurring/repeating value is assigned with a label. The label is placed instead of the numerical value in the entire program code.

60. The labels or constants that can be used by any module in the program is possible when they are declared as
a) PUBLIC
b) LOCAL
c) GLOBAL
d) Either PUBLIC or GLOBAL
View Answer
Answer: c
Explanation: The labels, constants, variables, procedures declared as GLOBAL can be used by any module in the program.

61. The stack pointer register contains
a) address of the stack segment
b) pointer address of the stack segment
c) offset of address of stack segment
d) data present in the stack segment
View Answer
Answer: c
Explanation: The stack pointer register contains the offset of the address of the stack segment.

62. The stack segment register contains
a) address of the stack segment
b) base address of the stack segment
c) pointer address of the stack segment
d) data in the stack segment
View Answer
Answer: b
Explanation: The stack segment register contains base address of the stack segment in the memory. The stack pointer register (sP) and stack segment register (SS) together address the stack-top.

63. PUSH operation
a) decrements SP
b) increments SP

c) decrements SS
d) increments SS
View Answer
Answer: a
Explanation: Each PUSH operation decrements the SP (Stack Pointer) register.

64. POP operation
a) decrements SP
b) increments SP
c) decrements SS
d) increments SS
View Answer
Answer: b
Explanation: Each POP operation increments the SP (Stack Pointer) register.

65. The register or memory location that is pushed into the stack at the end must be
a) popped off last
b) pushed off first
c) popped off first
d) pushed off last
View Answer
Answer: c
Explanation: The data can be retrieved by POP operation and as in stack, the data that is pushed at the end must be popped off first.

66. While CPU is executing a program, an interrupt exists then it
a) follows the next instruction in the program
b) jumps to instruction in other registers
c) breaks the normal sequence of execution of instructions
d) stops executing the program
View Answer
Answer: c
Explanation: An interrupt function is to break the sequence of operation.

67. An interrupt breaks the execution of instructions and diverts its execution to
a) Interrupt service routine
b) Counter word register
c) Execution unit
d) control unit
View Answer
Answer: a
Explanation: An interrupt transfers the control to interrupt service routine (ISR). After executing ISR, the control is transferred back again to the main program.

68. While executing the main program, if two or more interrupts occur, then the sequence of appearance of interrupts is called
a) multi-interrupt
b) nested interrupt
c) interrupt within interrupt

d) nested interrupt and interrupt within interrupt
View Answer
Answer: d
Explanation: If an interrupt occurs while executing a program, and the processor is executing the interrupt, if one more interrupt occurs again, then it is called a nested interrupt.

69. Whenever a number of devices interrupt a CPU at a time, and if the processor is able to handle them properly, it is said to have
a) interrupt handling ability
b) interrupt processing ability
c) multiple interrupt processing ability
d) multiple interrupt executing ability
View Answer
Answer: c
Explanation: The processor if handles more devices as interrupts then it has multiple interrupt processing ability.

70. NMI stands for
a) nonmaskable interrupt
b) nonmultiple interrupt
c) nonmovable interrupt
d) none of the mentioned
View Answer
Answer: a
Explanation: NMI is the acronym for nonmaskable interrupt.

71. If any interrupt request given to an input pin cannot be disabled by any means then the input pin is called
a) maskable interrupt
b) nonmaskable interrupt
c) maskable interrupt and nonmaskable interrupt
d) none of the mentioned
View Answer
Answer: b
Explanation: A nonmaskable interrupt input pin is one which means that any interrupt request at NMI (nonmaskable interrupt) input cannot be masked or disabled by any means.

71. The INTR interrupt may be
a) maskable
b) nonmaskable
c) maskable and nonmaskable
d) none of the mentioned
View Answer
Answer: a
Explanation: the INTR (interrupt request) is maskable or can be disabled.

73. The Programmable interrupt controller is required to
a) handle one interrupt request
b) handle one or more interrupt requests at a time

c) handle one or more interrupt requests with a delay
d) handle no interrupt request
View Answer
Answer: b
Explanation: If more than one interrupt request (INTR) occurs at a time, then an external chip called programmable interrupt controller is required to handle them.

74. The INTR interrupt may be masked using the flag
a) direction flag
b) overflow flag
c) interrupt flag
d) sign flag
View Answer
Answer: c
Explanation: If a microprocessor wants to serve any interrupt then interrupt flag, IF=1. If interrupt flag, IF=0, then the processor ignores the service.

75. If an interrupt is generated from outside the processor then it is an
a) internal interrupt
b) external interrupt
c) interrupt
d) none of the mentioned
View Answer
Answer: b
Explanation: If an external device or a signal interrupts the processor from outside then it is an external interrupt.

76. If the interrupt is generated by the execution of an interrupt instruction then it is
a) internal interrupt
b) external interrupt
c) interrupt-in-interrupt
d) none of the mentioned
View Answer
Answer: a
Explanation: The internal interrupt is generated internally by the processor circuit or by the execution of an interrupt instruction.

77. Example of an external interrupt is
a) divide by zero interrupt
b) keyboard interrupt
c) overflow interrupt
d) type2 interrupt
View Answer
Answer: b
Explanation: Since the keyboard is external to the processor, it is an external interrupt.

78. Example of an internal interrupt is
a) divide by zero interrupt
b) overflow interrupt
c) interrupt due to INT

d) all of the mentioned
View Answer
Answer: d
Explanation: Since the interrupts occur within the processor itself, they are called internal interrupts.

79. The interrupt request that is independent of IF flag is
a) NMI
b) TRAP
c) Divide by zero
d) All of the mentioned
View Answer
Answer: d
Explanation: These requests are independent of IF flag.

80. The device that enables the microprocessor to read data from the external devices is
a) printer
b) joystick
c) display
d) reader
View Answer
Answer: b
Explanation: Since joystick is an input device, it reads data from the external devices.

81. The example of output device is
a) CRT display
b) 7-segment display
c) Printer
d) All of the mentioned
View Answer
Answer: d
Explanation: The output device transfers data from the microprocessor to the external devices.

82. The input and output operations are respectively similar to the operations,
a) read, read
b) write, write
c) read, write
d) write, read
View Answer
Answer: c
Explanation: The input activity is similar to read operation and the output activity is similar to write operation.

83. The operation, IOWR (active low) performs
a) write operation on input data
b) write operation on output data
c) read operation on input data
d) read operation on output data
View Answer

Answer: b
Explanation: IOWR (active low) operation means writing data to an output device and not an input device.

84. The latch or IC 74LS373 acts as
a) good input port
b) bad input port
c) good output port
d) bad output port
View Answer
Answer: c
Explanation: If the output port is to source large currents, the port lines must be buffered. So, the latch is used as it acts as a good output port.

85. Programmable peripheral input-output port is another name for
a) serial input-output port
b) parallel input-output port
c) serial input port
d) parallel output port
View Answer
Answer: b
Explanation: The parallel input-output port chip 8255 is also known as programmable peripheral input-output port.

86. Port C of 8255 can function independently as
a) input port
b) output port
c) either input or output ports
d) both input and output ports
View Answer
Answer: c
Explanation: Port C can function independently either as input or as output ports.

87. All the functions of the ports of 8255 are achieved by programming the bits of an internal register called
a) data bus control
b) read logic control
c) control word register
d) none of the mentioned
View Answer
Answer: c
Explanation: By programming the bits of control word register, the operations of the ports are specified.

88. The data bus buffer is controlled by
a) control word register
b) read/write control logic
c) data bus
d) none of the mentioned
View Answer

Answer: b
Explanation: The data bus buffer is controlled by read/write control logic.

89. The input provided by the microprocessor to the read/write control logic is
a) RESET
b) A1
c) WR(ACTIVE LOW)
d) All of the mentioned
View Answer
Answer: d
Explanation: RD(ACTIVE LOW), WR(ACTIVE LOW), A1, A0, RESET are the inputs provided by the microprocessor to the read/write control logic of 8255.

90. The device that receives or transmits data upon the execution of input or output instructions by the microprocessor is
a) control word register
b) read/write control logic
c) 3-state bidirectional buffer
d) none of the mentioned
View Answer
Answer: c
Explanation: 3-state bidirectional buffer is used to receives or transmits data upon the execution of input or output instructions by the microprocessor.

91. The port that is used for the generation of handshake lines in mode 1 or mode 2 is
a) port A
b) port B
c) port C Lower
d) port C Upper
View Answer
Answer: d
Explanation: Port C upper is used for the generation of handshake lines in mode 1 or mode 2.

92. If A1=0, A0=1 then the input read cycle is performed from
a) port A to data bus
b) port B to data bus
c) port C to data bus
d) CWR to data bus
View Answer
Answer: b
Explanation: If A1=0, A0=1 then the input read cycle is performed from port B to data bus.

93. The function, ‘data bus tristated’ is performed when
a) CS(active low) = 1
b) CS(active low) = 0
c) CS(active low) = 0, RD(active low) = 1, WR(active low) = 1
d) CS(active low) = 1 OR CS(active low) = 0, RD(active low) = 1, WR(active low) = 1
View Answer

Answer: d
Explanation: The data bus is tristated when chip select pin=1 or chip select pin=0 and read and write signals are high i.e 1.

94. The pin that clears the control word register of 8255 when enabled is
a) CLEAR
b) SET
c) RESET
d) CLK
View Answer
Answer: c
Explanation: If reset pin is enabled then the control word register is cleared.

95. In the I/O mode, the 8255 ports work as
a) reset pins
b) set pins
c) programmable I/O ports
d) only output ports
View Answer
Answer: c
Explanation: In the I/O mode, the 8255 ports work as programmable I/O ports.

96. In BSR mode, only port C can be used to
a) set individual ports
b) reset individual ports
c) set and reset individual ports
d) programmable I/O ports
View Answer
Answer: c
Explanation: In BSR (Bit Set-Reset) Mode, port C can be used to set and reset its individual port bits.

97. The feature of mode 0 is
a) any port can be used as input or output
b) output ports are latched
c) maximum of 4 ports are available
d) all of the mentioned
View Answer
Answer: d
Explanation: In mode 0, any port can be used as input or output and output ports are latched.

98. The strobed input/output mode is another name of
a) mode 0
b) mode 1
c) mode 2
d) none
View Answer

Answer: b
Explanation: In this mode, the handshaking signals control the input or output action of the specified port.

99. If the value of the pin STB (Strobe Input) falls to low level, then
a) input port is loaded into input latches
b) input port is loaded into output latches
c) output port is loaded into input latches
d) output port is loaded into output latches
View Answer
Answer: a
Explanation: If the value of the pin STB (Strobe Input) falls to low level, the input port is loaded into input latches.

100. DAC (Digital to Analog Converter) finds application in
a) digitally controlled gains
b) motor speed controls
c) programmable gain amplifiers
d) all of the mentioned
View Answer
Answer: d
Explanation: DAC is used in digitally controlled gains, motor speed controls and programmable gain amplifiers.

102. To save the DAC from negative transients the device connected between OUT1 and OUT2 of AD 7523 is
a) p-n junction diode
b) Zener
c) FET
d) BJT (Bipolar Junction transistor)
View Answer
Answer: b
Explanation: Zener is connected between OUT1 and OUT2 pins of AD7523 to save from negative transients.

103. An operational amplifier connected to the output of AD 7523 is used
a) to convert current output to output voltage
b) to provide additional driving capability
c) as current-to-voltage converter
d) all of the mentioned
View Answer
Answer: d
Explanation: An operational amplifier is used as a current-to-voltage converter to convert the current output to output voltage and also provides additional driving capability to the DAC.

104. The DAC 0800 has a settling time of
a) 100 milliseconds
b) 100 microseconds
c) 50 milliseconds

d) 50 microseconds
View Answer
Answer: a
Explanation: DAC 0800 has a settling time of 100 milliseconds.

105. The device that is used to obtain an accurate position control of rotating shafts in terms of steps is
a) DC motor
b) AC motor
c) Stepper motor
d) Servo motor
View Answer
Answer: c
Explanation: Stepper motor employs rotation of its shaft in terms of steps, rather than continuous rotation as in case of AC or DC motors.

106. The number of counters that are present in the programmable timer device 8254 is
a) 1
b) 2
c) 3
d) 4
View Answer
Answer: c
Explanation: There are three counters that can be used as either counters or delay generators.

107. The operation that can be performed on control word register is
a) read operation
b) write operation
c) read and write operations
d) none
View Answer
Answer: b
Explanation: The control word register can only be written and cannot be read.

108. The mode that is used to interrupt the processor by setting a suitable terminal count is
a) mode 0
b) mode 1
c) mode 2
d) mode 3
View Answer
Answer: a
Explanation: Mode 0 is also called as an interrupt on the terminal count.

109. In mode 2, if N is loaded as the count value, then after (N-1) cycles, the output becomes low for
a) 1 clockcycle
b) 2 clockcycles
c) 3 clockcycles

d) 4 clockcycles
View Answer
Answer: a
Explanation: After (N-1) cycles, the output becomes low for only 1 clockcycle. If the count N is reloaded and again the output becomes high and remains so for (N-1) clock pulses.

110. The generation of a square wave is possible in the mode
a) mode 1
b) mode 2
c) mode 3
d) mode 4
View Answer
Answer: c
Explanation: When the count N loaded is even, then for half of the count, the output remains high and for the remaining half it remains low. If the count loaded is odd, the first clock pulse decrements it by 1 resulting in an even count value.

111. In control word register, if SC1=0 and SC0=1, then the counter selected is
a) counter 0
b) counter 1
c) counter 2
d) none
View Answer
Answer: b
Explanation: SC denotes select counter.

112. In control word format, if RL1=1, RL0=1 then the operation performed is
a) read/load least significant byte only
b) read/load most significant byte only
c) read/load LSB first and then MSB
d) read/load MSB first and then LSB
View Answer
Answer: c
Explanation: To access 16 bit, first LSB is loaded first, and then MSB.

113. If BCD=0, then the operation is
a) decimal count
b) hexadecimal count
c) binary count
d) octal count
View Answer
Answer: b
Explanation: If BCD=0 then hexadecimal count. If BCD=1, then the operation is BCD count.

114. The counter starts counting only if
a) GATE signal is low
b) GATE signal is high
c) CLK signal is low
d) CLK signal is high
View Answer

Answer: b
Explanation: If the GATE signal is enabled, then the counter starts counting.

115. The control word register contents are used for
a) initializing the operating modes
b) selection of counters
c) choosing binary/BCD counters
d) all of the mentioned
View Answer
Answer: d
Explanation: The control word register contents are used for
i) initializing the operating modes (mode 0-mode 4)
ii) selection of counters (counter0-counter2)
iii) choosing binary or BCD counters
iv) loading of the counter registers.

116. The number of hardware interrupts that the processor 8085 consists of is
a) 1
b) 3
c) 5
d) 7
View Answer
Answer: c
Explanation: The processor 8085 has five hardware interrupt pins. Out of these five, four pins were alloted fixed vector addresses but the pin INTR was not alloted by vector address, rather an external device was supposed to hand over the type of the interrupt to the microprocessor.

117. The register that stores all the interrupt requests in it in order to serve them one by one on a priority basis is
a) Interrupt Request Register
b) In-Service Register
c) Priority resolver
d) Interrupt Mask Register
View Answer
Answer: a
Explanation: The interrupts at IRQ input lines are handled by Interrupt Request Register internally.

118. The register that stores the bits required to mask the interrupt inputs is
a) In-service register
b) Priority resolver
c) Interrupt Mask register
d) None
View Answer
Answer: c
Explanation: Also, Interrupt Mask Register operates on IRR(Interrupt Request Register) at the direction of the Priority Resolver.

119. The interrupt control logic
a) manages interrupts
b) manages interrupt acknowledge signals
c) accepts interrupt acknowledge signal
d) all of the mentioned
View Answer
Answer: d
Explanation: The interrupt control logic performs all the operations that are involved within the interrupts like accepting and managing interrupt acknowledge signals, interrupts.

120. In a cascaded mode, the number of vectored interrupts provided by 8259A is
a) 4
b) 8
c) 16
d) 64
View Answer
Answer: d
Explanation: A single 8259A provides 8 vectored interrupts. In cascade mode, 64 vectored interrupts can be provided.

121. When the PS(active low)/EN(active low) pin of 8259A used in buffered mode, then it can be used as a
a) input to designate chip is master or slave
b) buffer enable
c) buffer disable
d) none
View Answer
Answer: b
Explanation: When the pin is used in buffered mode, then it can be used as a buffer enable to control buffer transreceivers. If it is not used in buffered mode, then the pin is used as input to designate whether the chip is used as a master or a slave.

122. Once the ICW1 is loaded, then the initialization procedure involves
a) edge sense circuit is reset
b) IMR is cleared
c) slave mode address is set to 7
d) all of the mentioned
View Answer
Answer: d
Explanation: The initialization procedure involves
i) edge sense circuit is reset.
ii) IMR is cleared.
iii) IR7 input is assigned the lowest priority.
iv) slave mode address is set to 7
v) special mask mode is cleared and the status read is set to IRR.

123. When non-specific EOI command is issued to 8259A it will automatically
a) set the ISR
b) reset the ISR

c) set the INTR
d) reset the INTR
View Answer
Answer: b
Explanation: When non-specific EOI command is issued to 8259A it will automatically reset the highest ISR.

124. In the application where all the interrupting devices are of equal priority, the mode used is
a) Automatic rotation
b) Automatic EOI mode
c) Specific rotation
d) EOI
View Answer
Answer: a
Explanation: The automatic rotation is used in the applications where all the interrupting devices are of equal priority.

125. Which of the following is not a mode of data transmission?
a) simplex
b) duplex
c) semi duplex
d) half duplex
View Answer
Answer: c
Explanation: Basically, there are three modes of data transmission. simplex, duplex and half duplex.

126. If the data is transmitted only in one direction over a single communication channel, then it is of
a) simplex mode
b) duplex mode
c) semi duplex mode
d) half duplex mode
View Answer
Answer: a
Explanation: In simplex mode, the data transmission is unidirectional. For example, a CPU may transmit data for a CRT display unit in this mode.

127. If the data transmission takes place in either direction, but at a time data may be transmitted only in one direction then, it is of
a) simplex mode
b) duplex mode
c) semi duplex mode
d) half duplex mode
View Answer
Answer: d
Explanation: In half duplex mode, data transmission is bidirectional but not at a time. For example, Walkie-Talkie.

128. In 8251A, the pin that controls the rate at which the character is to be transmitted is
a) TXC(active low)
b) TXC(active high)
c) TXD(active low)
d) RXC(active low)
View Answer
Answer: a
Explanation: Transmitter Clock Input (TXC(active low)) is a pin that controls the rate at which the character is to be transmitted.

129. TXD(Transmitted Data Output) pin carries serial stream of the transmitted data bits along with
a) start bit
b) stop bit
c) parity bit
d) all of the mentioned
View Answer
Answer: d
Explanation: Transmitted Data Output pin carries a serial stream of the transmitted data bits along with other information like start bits, stop bits and parity bits etc.

130. The signal that may be used either to interrupt the CPU or polled by the CPU is
a) TXRDY(Transmitter ready)
b) RXRDY(Receiver ready output)
c) DSR(active low)
d) DTR(active low)
View Answer
Answer: b
Explanation: RXRDY(Receiver ready output) may be used either to interrupt the CPU or polled by the CPU.

131. The disadvantage of RS-232C is
a) limited speed of communication
b) high-voltage level signaling
c) big-size communication adapters
d) all of the mentioned
View Answer
Answer: d
Explanation: RS232C has been used for long and has a few disadvantages like limited speed of communication, high-voltage level signaling and big-size communication adapters.

132. The USB supports the signaling rate of
a) full-speed USB 1.0 at rate of 12 Mbps
b) high-speed USB 2.0 at rate of 480 Mbps
c) super-speed USB 3.0 at rate of 596 Mbps
d) all of the mentioned
View Answer

Answer: d
Explanation: The USB standards support the signaling rates. Also, USB signaling is implemented in a differential in low- and full-speed options.

133. The bit packet that commands the device either to receive data or transmit data in transmission of USB asynchronous communication is
a) Handshake packet
b) Token packet
c) PRE packet
d) Data packet
View Answer
Answer: b
Explanation: The token packet is the second type of packet which commands the device either to receive data or transmit data.

134. High speed USB devices neglect
a) Handshake packet
b) Token packet
c) PRE packet
d) Data packet
View Answer
Answer: c
Explanation: PRE packets are only of importance to low-speed USB devices.

135. The registers that store the keyboard and display modes and operations programmed by CPU are
a) I/O control and data buffers
b) Control and timing registers
c) Return buffers
d) Display address registers
View Answer
Answer: b
Explanation: The control and timing register to store the keyboard and display modes and other operations programmed by CPU.

136. The sensor RAM acts as 8-byte first-in-first-out RAM in
a) keyboard mode
b) strobed input mode
c) keyboard and strobed input mode
d) scanned sensor matrix mode
View Answer
Answer: c
Explanation: In this mode, each key code of the pressed key is entered in the order of the entry, and in the meantime, read by the CPU, till the RAM becomes empty.

137. The registers that hold the address of the word currently being written by the CPU from the display RAM are
a) control and timing register
b) control and timing register and timing control
c) display RAM

d) display address registers
View Answer
Answer: d
Explanation: The display address registers holds the address of the word currently being written or read by the CPU to or from the display RAM.

138. When a key is pressed, a debounce logic comes into operation in
a) scanned keyboard special error mode
b) scanned keyboard with N-key rollover
c) scanned keyboard mode with 2 key lockout
d) sensor matrix mode
View Answer
Answer: c
Explanation: In scanned keyboard mode with 2 key lockout mode of operation, when a key is pressed, a debounce logic comes into operation. During the next two scans, other keys are checked for closure and if no other key is pressed then the first pressed key is identified.

139. The mode that is programmed using “end interrupt/error mode set command” is
a) scanned keyboard special error mode
b) scanned keyboard with N-key rollover
c) scanned keyboard mode with 2 key lockout
d) sensor matrix mode
View Answer
Answer: a
Explanation: The scanned keyboard special error mode is programmed using end interrupt/error mode set command. This mode is valid only under the N-key rollover mode.

140. The 80286 is able to address the physical memory of
a) 8 MB
b) 16 MB
c) 24 MB
d) 64 MB
View Answer
Answer: b
Explanation: The 80286 with its 24-bit address bus is able to address 16 Mbytes of physical memory.

142. The 80286 is able to operate with the clock frequency of
a) 12.5 MHz
b) 10 MHz
c) 8 MHz
d) all of the mentioned
View Answer
Answer: d
Explanation: Various versions of 80286 are available that run on 12.5 MHz, 10 MHz and 8 MHz clock frequencies.

143. The management of the memory system required to ensure the smooth execution of the running process is done by

a) control unit
b) memory
c) memory management unit
d) bus interface unit
View Answer
Answer: c
Explanation: The memory management which is an important task of the operating system is now supported by a hardware unit called a memory management unit.

144. The fetching of the program from secondary memory to place it in physical memory, during the execution of CPU is called
a) mapping
b) swapping in
c) swapping out
d) pipelining
View Answer
Answer: b
Explanation: Whenever the portion of a program is required for execution by the CPU, it is fetched from the secondary memory and placed in the physical memory. This is called swapping in of the program.

145. The process of making the physical memory free by storing the portion of program and partial results in the secondary storage called
a) mapping
b) swapping in
c) swapping out
d) pipelining
View Answer
Answer: c
Explanation: In swapping out, a portion of the program or important partial results required for further execution, may be saved back on secondary storage to make the physical memory free, for further execution of another required portion of the program.

146. The memory that is considered as a large logical memory space, that is not available physically is
a) logical memory
b) auxiliary memory
c) imaginary memory
d) virtual memory
View Answer
Answer: d
Explanation: To the user, there exists a very large logical memory space, which is actually not available called virtual memory. This does not exist physically in a system. It is however, possible to map a large virtual memory space onto the real physical memory.

147. The memory management and protection mechanisms are enabled with advanced instruction set when 80286 is operated in
a) normal mode
b) real address mode

c) virtual address mode
d) all of the mentioned
View Answer
Answer: c
Explanation: In virtual address mode, 80286 works with all of its memory management and protection capabilities, with the advanced instruction set.

148. The 80286 is an upward object code compatible with 8086 or 8088 when operated in
a) normal mode
b) real address mode
c) virtual address mode
d) real and virtual address mode
View Answer
Answer: d
Explanation: The 80286 is operated in two modes, namely real address mode and virtual address mode. In both the modes, the 80286 is compatible with 8086/8088.

149. The CPU of 80286 contains
a) 16-bit general purpose registers
b) 16-bit segment registers
c) status and control register
d) all of the mentioned
View Answer
Answer: d
Explanation: The CPU of 80286 contains the same set of registers as in 8086.

150. The additional field that is available in 80286 is
a) I/O Privilege field
b) nested task flag
c) protection enable
d) all of the mentioned
View Answer
Answer: d
Explanation: The additional fields available in 80286 flag register are, I/O Privilege field, nested task flag, protection enable, and monitor processor extension.

151. Which of the block is not considered as a block of an architecture of 80286?
a) address unit
b) bus unit
c) instruction unit
d) control unit
View Answer
Answer: d
Explanation: The CPU may be viewed to contain four functional parts and they are
i) Address Unit
ii) Bus Unit
iii) Instruction Unit
iv) Execution Unit.

151. The 80386DX is a processor that supports
a) 8-bit data operand
b) 16-bit data operand
c) 32-bit data operand
d) all of the mentioned
View Answer
Answer: d
Explanation: The 80386DX is a 32-bit processor that supports, 8-bit/16-bit/32-bit data operands.

152. The 80386DX has an address bus of
a) 8 address lines
b) 16 address lines
c) 32 address lines
d) 64 address lines
View Answer
Answer: c
Explanation: The 80386, with its 32-bit address bus, can address up to 4 GB of physical memory.

153. The number of debug registers that are available in 80386, for hardware debugging and control is
a) 2
b) 4
c) 8
d) 16
View Answer
Answer: c
Explanation: The 80386 offers a set of total eight debug registers DR0-DR7, for hardware debugging and control.

154. The memory management of 80386 supports
a) virtual memory
b) paging
c) four levels of protection
d) all of the mentioned
View Answer
Answer: d
Explanation: The memory management section of 80386 supports the virtual memory, paging and four levels of protection, maintaining full compatibility with 80286.

155. The 80386 enables itself to organize the available physical memory into pages, which is known as
a) segmentation
b) paging
c) memory division
d) none of the mentioned
View Answer

Answer: b
Explanation: The concept of paging which is introduced in 80386, enables it to organize the available physical memory into pages of size 4 KB each, under the segmented memory.

156. The architecture of 8051 consists of
a) 4 latches
b) 2 timer registers
c) 4 on-chip I/O ports
d) all of the mentioned
View Answer
Answer: d
Explanation: The architecture of 8051 consists of 4 latches and driver pairs are allotted to each of the four on-chip I/O ports. It contains two 16-bit timer registers.

157. Which of the following is an 8-bit register?
a) PSW(Program Status Word)
b) TCON(Timer Control Register)
c) Accumulator
d) All of the mentioned
View Answer
Answer: d
Explanation: The registers, PSW, TCON and Accumulator are 8-bit registers.

158. Which of the following register can be addressed as a byte?
a) P1
b) SCON
c) TMOD
d) TCON
View Answer
Answer: c
Explanation: The registers, TMOD, SP, TH0, TH1, TL0, TL1 are to be addressed as bytes.

159. Which of the following is bit-addressable register?
a) SBUF
b) PCON
c) TMOD
d) SCON
View Answer
Answer: d
Explanation: The registers, accumulator, PSW, B, P0, P1, P2, P3, IP, IE, TCON and SCON are all bit-addressable registers.

160. The higher and lower bytes of a 16-bit register DPTR are represented respectively as
a) LDPTR and HDPTR
b) DPTRL and DPTRH
c) DPH and DPL
d) HDP and LDP
View Answer

Answer: c
Explanation: The registers, DPH and DPL are the higher and lower bytes of a 16-bit register DPTR.

161. The register that is used for accessing external data memory is
a) DPH
b) DPL
c) DPTR
d) NONE
View Answer
Answer: c
Explanation: The Data Pointer(DPTR) is used for accessing external data memory which means that it includes both DPH and DPL.

162. The number of 8-bit registers that a register bank contain is
a) 2
b) 4
c) 6
d) 8
View Answer
Answer: d
Explanation: The 32, 8-bit registers are divided into four groups of 8 registers each, called register banks.

163. If RS1=1, RS0=0, then the register bank selected is
a) register bank 0
b) register bank 1
c) register bank 2
d) register bank 3
View Answer
Answer: c
Explanation: If RS1=1, RS0=0, then the register bank selected is register bank 2.

164. If RS1=1, RS0=1, then the register bank selected is
a) register bank 0
b) register bank 1
c) register bank 2
d) register bank 3
View Answer
Answer: d
Explanation: If RS1=1, RS0=1, then the register bank selected is register bank 3. If RS1=0, RS0=0, then selected bank is register bank 0.

165. The PCON register consists of
a) power mode bit
b) power idle bit
c) power ideal bit
d) power down bit and idle bit
View Answer

Answer: d
Explanation: The power control register, PCON consists of power down bit and idle bit which activate the power down mode and idle mode in 80C51BH.

166. The on-chip oscillator is stopped in
a) power mode
b) power down mode
c) idle mode
d) ideal mode
View Answer
Answer: b
Explanation: In power down mode, the on-chip oscillator is stopped.

167. In idle mode, the device that is disabled is
a) serial port
b) timer block
c) clock to CPU
d) all of the mentioned
View Answer
Answer: c
Explanation: In idle mode, the oscillator continues to run and the interrupt, serial port and timer blocks are active but the clock to the CPU is disabled.

168. The only way to terminate the power down mode is to
a) CLEAR
b) RESET
c) HOLD
d) HLT
View Answer
Answer: b
Explanation: The only way to terminate the power down mode is hardware reset. The reset redefines all the SFRs but the RAM contents are left unchanged.

169. The idle mode can be terminated by
a) PRESET
b) CLEAR
c) Interrupt
d) Interrupt or reset
View Answer
Answer: d
Explanation: The idle mode can be terminated with a hardware interrupt or hardware reset signal.

170. Which of the following is an external interrupt?
a) INT0(active low)
b) INT2(active low)
c) Timer0 interrupt
d) Timer1 interrupt
View Answer

Answer: a
Explanation: INT0(active low) and INT1(active low) are two external interrupt inputs provided by 8051.

171. The interrupts, INT0(active low) and INT1(active low) are processed internally by flags
a) IE0 and IE1
b) IE0 and IF1
c) IF0 and IE1
d) IF0 and IF1
View Answer
Answer: a
Explanation: The interrupts, INT0(active low) and INT1(active low) are processed internally by the flags IE0 and IE1.

172. The flags IE0 and IE1, are automatically cleared after the control is transferred to respective vector if the interrupt is
a) level-sensitive
b) edge-sensitive
c) in serial port
d) in parallel port
View Answer
Answer: b
Explanation: If the interrupts are programmed as edge sensitive, the flags IE0 and IE1 are automatically cleared after the control is transferred to respective vector.

173. If the external interrupt sources control the flags IE0 and IE1, then the interrupt programmed is
a) level-sensitive
b) edge-sensitive
c) in serial port
d) in parallel port
View Answer
Answer: a
Explanation: If the interrupts are programmed as level sensitive, then the flags IE0 and IE1 are controlled by external interrupt sources themselves.

174. The pulses at T0 or T1 pin are counted in
a) timer mode
b) counter mode
c) idle mode
d) power down mode
View Answer
Answer: b
Explanation: In counter mode, the pulses are counted at T0 or T1 pin.

175. Which of the following is not an addressing mode of 8051?
a) register instructions
b) register specific instructions
c) indexed addressing

d) none
View Answer
Answer: d
Explanation: The six addressing modes of 8051 are
1. Direct addressing
2. Indirect addressing
3. Register instructions
4. Register specific(Register Implicit) instructions
5. Immediate mode
6. Indexed addressing.

176. The symbol, ‘addr 16’ represents the 16-bit address which is used by the instructions to specify the
a) destination address of CALL
b) source address of JUMP
c) destination address of call or jump
d) source address of call or jump
View Answer
Answer: c
Explanation: The symbol, ‘addr 16’ represents the 16-bit destination address which is used by the LCALL or LJMP instruction to specify the call or jump destination address, within 64 Kbytes program memory.

177. The storage of addresses that can be directly accessed is
a) external data RAM
b) internal data ROM
c) internal data RAM and SFRS
d) external data ROM and SFRS
View Answer
Answer: c
Explanation: Only internal data RAM and SFRS can be directly addressed in direct addressing mode.

178. The address register for storing the 16-bit addresses can only be
a) stack pointer
b) data pointer
c) instruction register
d) accumulator
View Answer
Answer: b
Explanation: The address register for storing the 16-bit addresses can only be data pointer.

179. The address register for storing the 8-bit addresses can be
a) R0 of the selected bank of register
b) R1 of the selected bank of register
c) Stack pointer
d) All of the mentioned
View Answer

Answer: d
Explanation: The registers R0 and R1 of the selected bank of registers or stack pointer can be used as address registers for storing the 8-bit addresses.

180. The instruction, ADD A, R7 is an example of
a) register instructions
b) register specific instructions
c) indexed addressing
d) none
View Answer
Answer: a
Explanation: In register instructions addressing mode, operands are stored in the registers R0-R7 of the selected register bank. One of these registers is specified in the instruction.

181. The addressing mode, in which the instructions has no source and destination operands is
a) register instructions
b) register specific instructions
c) direct addressing
d) indirect addressing
View Answer
Answer: b
Explanation: In register specific instructions addressing mode, the instructions don't have source and destination operands. Some of the instructions always operate only on a specific register.

182. The instruction, RLA performs
a) rotation of address register to left
b) rotation of accumulator to left
c) rotation of address register to right
d) rotation of accumulator to right
View Answer
Answer: b
Explanation: The instruction, RLA rotates accumulator left.

183. The instruction, ADD A, #100 performs
a) 100(decimal) is added to contents of address register
b) 100(decimal) is subtracted from the accumulator
c) 100(decimal) is added to contents of an accumulator
d) none
View Answer
Answer: c
Explanation: Immediate data 100(decimal) is added to the contents of the accumulator.

184. In which of these addressing modes, a constant is specified in the instruction, after the opcode byte?
a) register instructions
b) register specific instructions
c) direct addressing

d) immediate mode
View Answer
Answer: d
Explanation: In immediate mode, an immediate data, i.e. a constant is specified in the instruction, after the opcode byte.

185. The only memory which can be accessed using indexed addressing mode is
a) RAM
b) ROM
c) Main memory
d) Program memory
View Answer
Answer: d
Explanation: Only program memory can be accessed using the indexed addressing mode.

186. The data address of look-up table is found by adding the contents of
a) accumulator with that of program counter
b) accumulator with that of program counter or data pointer
c) data register with that of program counter or accumulator
d) data register with that of program counter or data pointer
View Answer
Answer: b
Explanation: The look-up table data address is found out by adding the contents of register accumulator with that of the program counter or data pointer.

187. Which of the following is not an instruction of 8051 instructions?
a) arithmetic instructions
b) boolean instructions
c) logical instructions
d) none
View Answer
Answer: d
Explanation: The 8051 instructions are categorized as
1. Data transfer instructions
2. Arithmetic instructions
3. Logical instructions
4. Boolean instructions
5. Control transfer instructions.

188. The operations performed by data transfer instructions are on
a) bit data
b) byte data
c) 16-bit data
d) all of the mentioned
View Answer
Answer: d
Explanation: The data transfer instructions implement a bit, byte, 16-bit data transfer operations between the SRC(source) and DST(destination) operands.

189. Which of the following is true while executing data transfer instructions?
a) program counter is not accessible
b) restricted bit-transfer operations are allowed
c) both operands can be direct/indirect register operands
d) all of the mentioned
View Answer
Answer: c
Explanation: In data transfer instructions,
1. Program counter is not accessible.
2. Restricted bit-transfer operations are allowed.
3. Both operands can be direct/indirect register operands.
4. BOth operands can be internal direct data memory operands.

190. The logical instruction that affects the carry flag during its execution is
a) XRL A;
b) ANL A;
c) ORL A;
d) RLC A;
View Answer
Answer: d
Explanation: The logical instructions that doesn’t affect the carry flag are, ANL, ORL and XRL. The logical instructions that affect the carry flag during its execution are RL, RLC, RRC and RR.

191. The instruction that is used to complement or invert the bit of a bit addressable SFR is
a) CLR C
b) CPL C
c) CPL Bit
d) ANL Bit
View Answer
Answer: c
Explanation: The instruction, CPL Bit is used to complement or invert the bit of a bit addressable SFR or RAM.

192. The external interrupts of 8051 can be enabled by
a) 4 LSBs of TCON register
b) Interrupt enable
c) priority register
d) all of the mentioned
View Answer
Answer: d
Explanation: The external interrupts namely INT0(active low) and INT1(active low) can be enabled and programmed using the least significant four bits of TCON register and the Interrupt enable and priority registers.

193. The bits that control the external interrupts are
a) ET0 and ET1
b) ET1 and ET2
c) EX0 and EX1

d) EX1 and EX2
View Answer
Answer: c
Explanation: The bits, EX0 and EX1 individually control the external interrupts, INT0(active low) and INT1(active low). If INT0(active low) and INT1(active low) interrupts are to be enabled then the bits EX0 and EX1 must be set respectively.

194. EA bit is used to
a) enable or disable external interrupts
b) enable or disable internal interrupts
c) enable or disable all the interrupts
d) none of the mentioned
View Answer
Answer: c
Explanation: Using EA bit, all the interrupts can be enabled or disabled. Using the individual respective bit, the respective interrupt can be enabled or disabled.

195. The number of priority levels that each interrupt of 8051 have is
a) 1
b) 2
c) 3
d) 4
View Answer
Answer: b
Explanation: Each interrupts level of 8051 can have two levels of priority namely level 0 and level 1. Level 1 is considered as a higher priority level compared to level 0.

196. The priority level of an interrupt of 8051 for which SI(serial interrupt) interrupt is programmed is
a) level 0
b) level 1
c) level 0 or level 1
d) none
View Answer
Answer: b
Explanation: SI interrupt is programmed for level 1 priority.