• Nouise	...g Time		

4.4.16 Converters–Analog to Digital (A/D) and Digital to Analog (D/A)

Module - IV

(i) Digital to Anlog Converter (DAC)

Analog output voltage V_A of an N-bit straight binary DAC converter is related to the digital equation

$$V_A = K(2^{N-1} b_{N-1} + 2^{N-2} b_{N-2} + \ldots + 2b_1 + b_0)$$

where K = proportionality factor

$$\left.\begin{aligned} b_j &= +1 \text{ if } j\text{th bit of input } 1 \\ &= 0 \text{ if } j\text{th bit of input is } 0 \end{aligned}\right\} j = 0 \text{ to } (N-1)$$

Weighted resistor DAC:

As the conversion D/A involves a weighted sum corresponding to the input to the converter, the summing circuit of Fig. 4.74 can be used as a DAC.

In this circuit, $I_i = I_{N-1} + I_{N-2} + \ldots + I_1 + I_0$

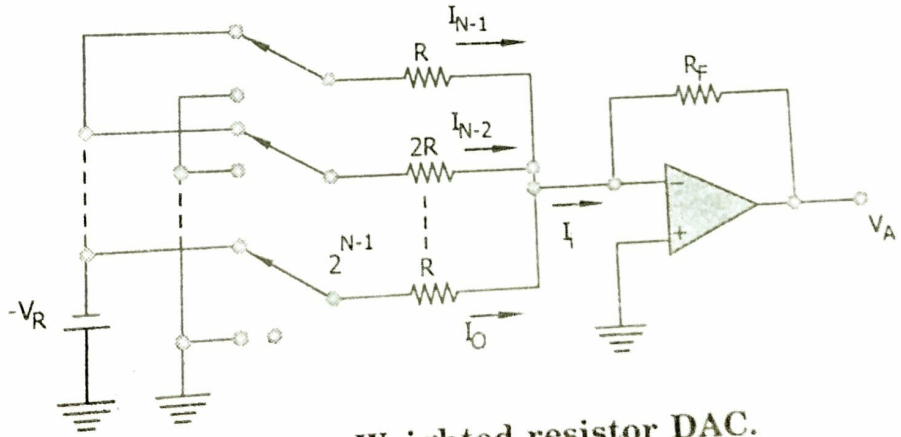


Fig. 4.72. Weighted resistor DAC.

These currents can be expressed in terms of voltages as

$$I_{N-1} = V_{N-1}/R$$
$$I_{N-2} = V_{N-2}/2R$$
$$\text{---} \quad \text{---}$$
$$\text{---} \quad \text{---}$$
$$I_0 = V_0/2^{N-1}R$$

Let $\quad V(0) = 0, \quad \text{and} \quad V(1) = -V_R$

Then $\quad V_N = -b_n V_R$

Switches in the circuit are digitally controlled causing b_n to acquire values 0 or 1.

Now,
$$I_i = -V_R\left[\frac{1}{R}b_{N-1} + \frac{1}{2R}b_{N-2} + \ldots + \frac{1}{2^{N-1}R}b_0\right]$$

The analog output of the circuit is given by

$$V_A = -R_F I_i$$
$$V_A = V_R\left[\frac{R_F}{R}b_{N-1} + \frac{R_F}{2R}b_{N-2} + \ldots + \frac{R_F}{2^{N-1}R}b_0\right]$$
$$= K[2^{N-1}b_{N-1} + 2^{N-1}b_{N-2} + \ldots + 2^1 b_1 + 2^0 b_0]$$

where $\quad K = \dfrac{R_F}{2^{N-1}R}$

Hence the circuit is a DAC.

R-2R ladder network:

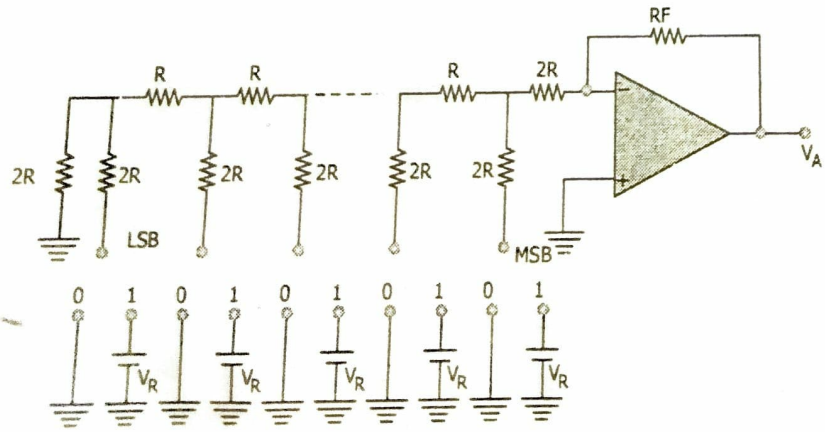
An R-2R ladder network [Fig. 4.75 *(a)*] uses resistors of only two values R and 2R. The inputs to the resistor network is applied through digitally controlled switches.

In a 3 bit R – 2 R ladder DAC [Fig. 4.75 *(a)*] the input is asumed as 001. Applying Thevenin's theorem at XX', YY' and ZZ' we obtain circuits of Figs. 4.75 *(a)*, *(b)* and *(c)* respectively. It is immediately seen that for input 001, voltage $V_R/2^3$ is applied through 3R to the inverting terminal of the OPAMP.

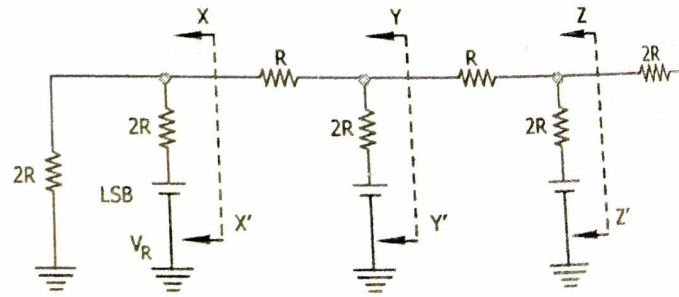
Similarly for the digital input of 010 and 100, the equivalent voltages are $V_R/2^2$ and $V_R/2^1$ respectively with resistance 3R in each case. Therefore, we get equivalent circuit of Fig. 4.76 *(d)* wherein the voltage V_0 is given by

$$V_0 = -\left[\frac{R_F}{3R}\frac{V_R}{2^3}b_0 + \frac{R_F}{3R}\frac{V_R}{2^2}b_1 + \frac{R_F}{3R}\frac{V_R}{2^1}b_2\right]$$
$$= -\left(\frac{R_F}{3R}\right)\left(\frac{V_R}{2^3}\right)\left[2^2 b_2 + 2^1 b_1 + 2^0 b_0\right]$$

This equation shows that analog output voltage is proportional to the digital input.



(a) R-2R tadder DAC network



(b) 3 bit R-2R ladder DAC network

Fig. 4.75

In general for N bit DAC.

$$V_0 = V\,[2^N b_{N-1} + 2^{N-2} b_{N-2} + \ldots + 2^1 b_1 + 2^0 b_0]$$

where $R_F = 3R$ and $V_R = -2^N V$

Number of resistors required for an N bit DAC

(*i*) In case of R–2R ladder is 2N

(*ii*) In case of weighted resistor network is N

But because of wide spread in the resistance values for large N, weighted resistor DAC is not widely used.

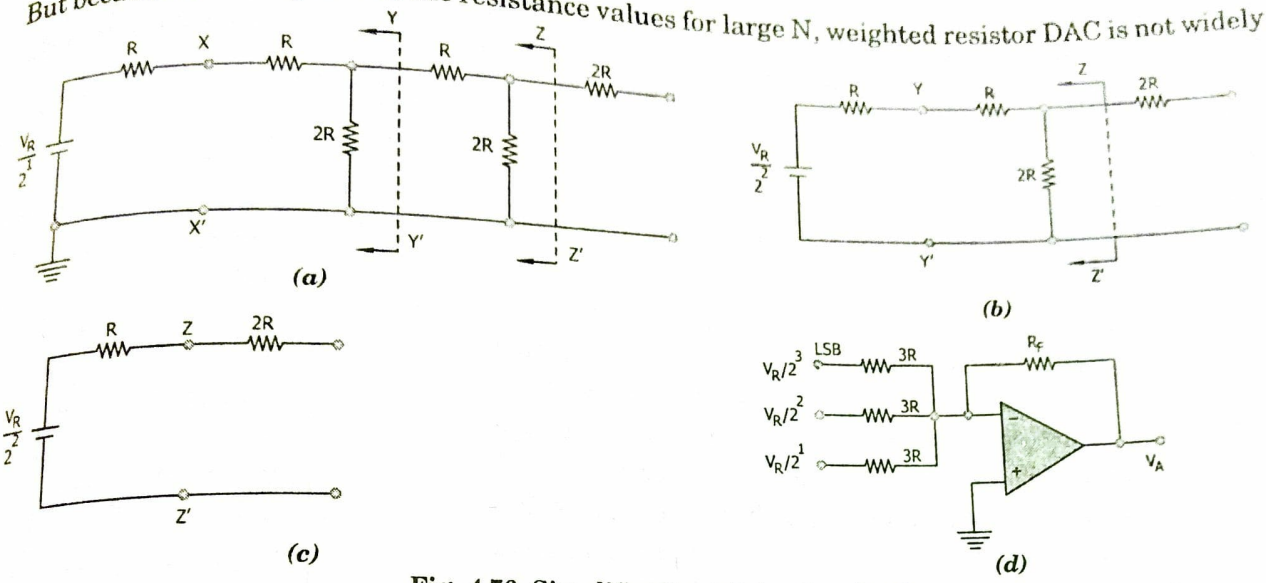


Fig. 4.76. Simplification of the circuit of

(*ii*) Analog to Digital Converter (ADC)

Counting ADC : This system is shown in Fig. 4.77 (*a*).

The clear pulse resets the counter to the zero count. The counter then records in binary form the number of pulses from the clock line. The clock is the source of pulses equally spaced in time. Since the number of pulses counted increases with time, the binary word representing this count is used as an input to the DAC, whose output is the staircase waveform shown in Fig. 4.77 (*b*). The comparator has an output which is 'HIGH' and the AND gate is open for transmission of clock pulses. When V_d exceeds V_a, the comparator output goes 'LOW' and AND gate is disabled. This stops the counting at the time when $V_a \approx V_d$ and the counter can be read as the digital output representing analog input voltage.

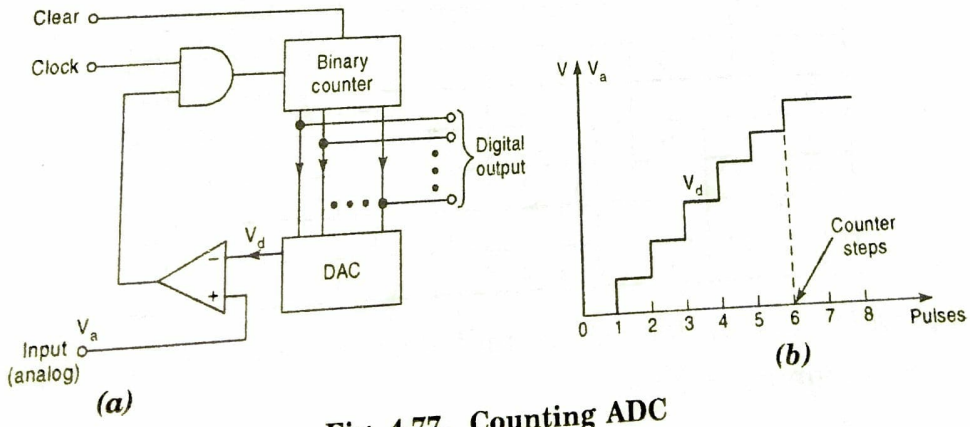


Fig. 4.77. Counting ADC

Module - V

8.13 SEMICONDUCTOR MEMORIES

Memory Organization and Operation

The basic element of a semiconductor memory is a FLIP - FLOP. The information is stored in bi There are a number of locations in a memory chip, each location being meant for one word information. The number of locations and the number of bits comprising the work vary from memory. The size of a memory chip is specified by two numbers M and N as N × N bits. The specifies the number of locations available in the memory and N is the number of bits at each In other words, this means that M words of N bits each can be stored in the memory. The com values of the number of words per chip are 64, 256, 512, 1024, 2048, 4096 etc. whereas the com for the number of words size are 1, 4 and 8 etc. Memories requiring higher number of words an word sizes can be formed by using these chips.

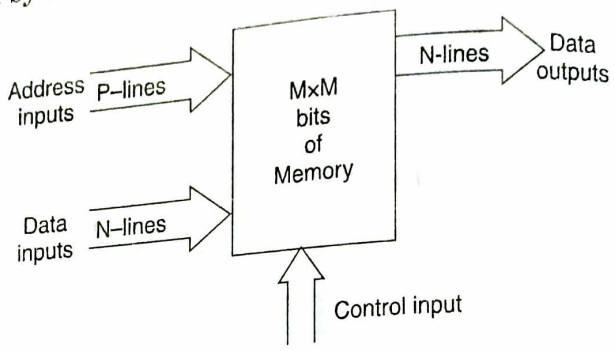


Fig. Block diagram of a memory device

Each of the M locations of the memory is defined by a unique address and therefore for accessin of the M locations, P inputs are required, where $2^P = M$. This set of lines is referred to as address i address bus. The address is specified in the binary form. For convenience, octal and hexa representations are commonly employed.

Most commonly used memories

1. **Sequentially accessed memory.**

   In the sequentially accessed memories, the memory location are accessed, for writing into or from in a sequential fashion. Therefore the time required for accessing a memory location (ref as access time) for writing into or reading from is different for different locations.

   Types. There are two types of sequentially accessed memories.

   (*i*) **Shift registers :** Shift registers can be either static or dynamic. In a static memory, the of the memory location do not change with time as long as power is on. On the other dynamic memories, the information is stored in MOS capacitors which changes with therefore it has to be refreshed at regular intervals. The dynamic memories are sim expensive, require less power have high packing density in comparison to static memorie therefore widely used in digital systems. However the cost of the additional circuitry re refreshing may increase the system cost.

   (*ii*) **Charge coupled devices (CCD) :** The charge coupled devices are implemented u technology. These devices have high density and low cost.

   The other mode of access of memory location is called as random-access in which the acc same for each memory location.

2. **Read only memory (ROM).**

   The read and write memories is a random-access memory and is referred to as RAM. RA static or dynamic.

3. **Read only memory (ROM).**

   It is meant only for reading the information from it.

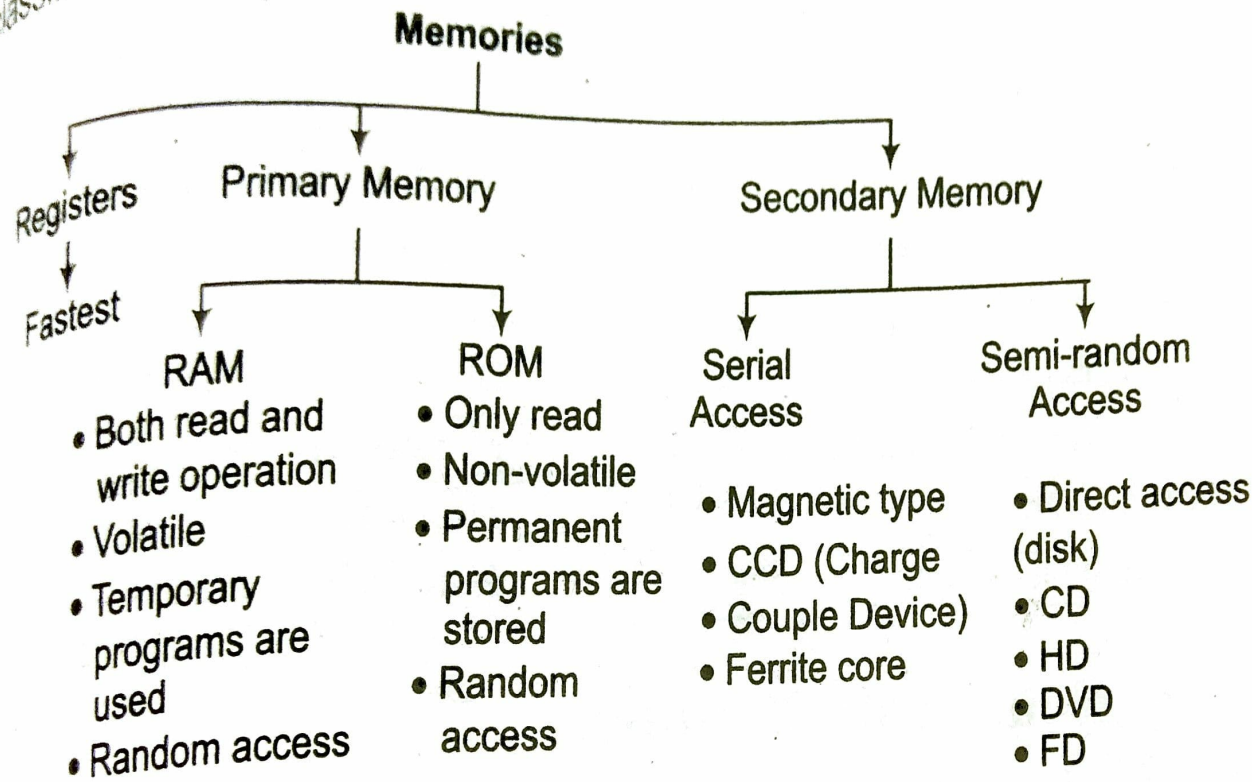
4. **Content addressable memory (CAM).**

   It is a special purpose random access memory which performs association operation in add write operation.

$t_{pd\,(FF)} + t_{pd\,(AND)}$

Memories

Memories are used in the computer to store the data. Memories are classified as



Classification of memories

Random Access Memory (RAM)

The time taken to transfer information to or from any desired location is always same hence it is called Random Access Memory (RAM).

$$2^n \times m \rightarrow \text{memory capacity}$$

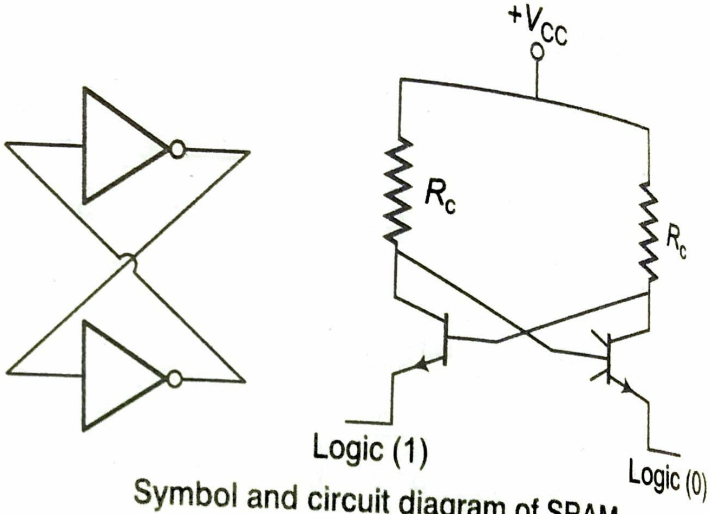
n : address line

m : data

Classification of RAM

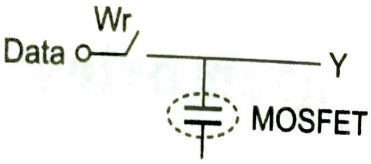
It is basically of two types

1. Static RAM



Symbol and circuit diagram of SRAM

2. Dynamic RAM



Circuit diagram of DRAM

Comparison between SRAM and DRAM

Static RAM	Dynamic RAM
Data is stored in flip flop like structure.	Data is stored in MOS capacity.
Can be implemented with BJT or MOSFET.	Only MOSFET is used.
Faster.	Slow.
Dissipate more power.	Dissipate less power.
Memory capacity is less.	Memory capacity is more.
Cache memory.	Main memory.
No refreshing required.	Refreshing is require.

ROM : Read Only Memory

- It is combinational circuit.
- It is also known as masked memory.

Comparison of Memories

ROM	Fixed	AND	Fixed	OR
PROM	Fixed	AND	Programmable	OR
PAL	Programable	AND	Fixed	OR
PLA	Programable	AND	Programable	OR