# SRINIX COLLEGE OF ENGINEERING

2nd INTERNAL EXAMINATION-2021-22

Subject-**DLD** Semester-3**RD** Branch-**CSE**

Full Mark-**100** Time-2.30Hrs

## PART-A

**ANSWER ALL THE QUESTIONS** **[2X10]**

**1.**

a) Convert$(133.6)_{10} = (?)_8$.
b) Find 2's complement of $(1101101)_2$ and $(26)_{10}$
c) Differentiate between combinational and sequential circuit.
d) Write about XOR and NOR.
e) Define flip-flop and its types.
f) Find the modulus, no of flip-flop and no of binary number for a 4-bit counter.
g) Draw a full adder using two half adders.
h) Differentiate between synchronous and asynchronous counter.
i) Define race around condition in flip-flop.
j) Write state diagram and state table of JK flip-flop.

**ANSWER ANY EIGHT PART-B** **[6×8=48]**

**2.**

a) Add (37) and (-56) in 2's compliment method.
b) (i) Given a message (1101).Find a 7bit Hamming code.
(ii) Define parity bit.
c) Given $Y = \sum m(0,1,3,5,6,10,14)$.Implement using a 4X1 MUX.
d) Given $Y = A + D$.Find the standard SOP format and min terms.
e) Explain the 4-bit synchronous up counter with diagram.
f) Describe about master-slave JK flip-flop.
g) Convert SR flip-flop to T flip-flop with diagram.
h) Explain about full substractor.
i) Design a decoder using full adder.
j) Describe about SR flip-flop with diagram and table.

**ANSWER ANY TWO** **PART-C** **[16×2]**

**3.** Given $Y = A\bar{B} + \bar{C}$
i) Draw using basic gates.
ii) Implement using only NAND gates
iii) Implement using only NOR gates.

**4.** Write short note on i) ASM chart ii) PISO shift register

**5.** Explain all about logic gates with its relevant information.

**----------ALL THE BEST----------**