

Microprocessor And Microcontroller (MPMC)

Semester - 5th

Branch - ETC (Module - IV)

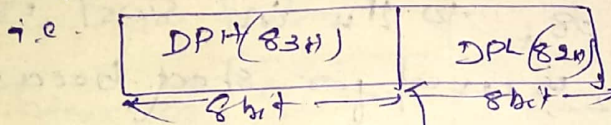
Short Questions :-

Q.1) What is the function of Data pointer (DPTR) in 8051?

A → The data pointer (DPTR) is a 16 bit register which consists of a high byte (DPH) and a low byte (DPL).

→ The function of DPTR is to hold a 16 bit external RAM address.

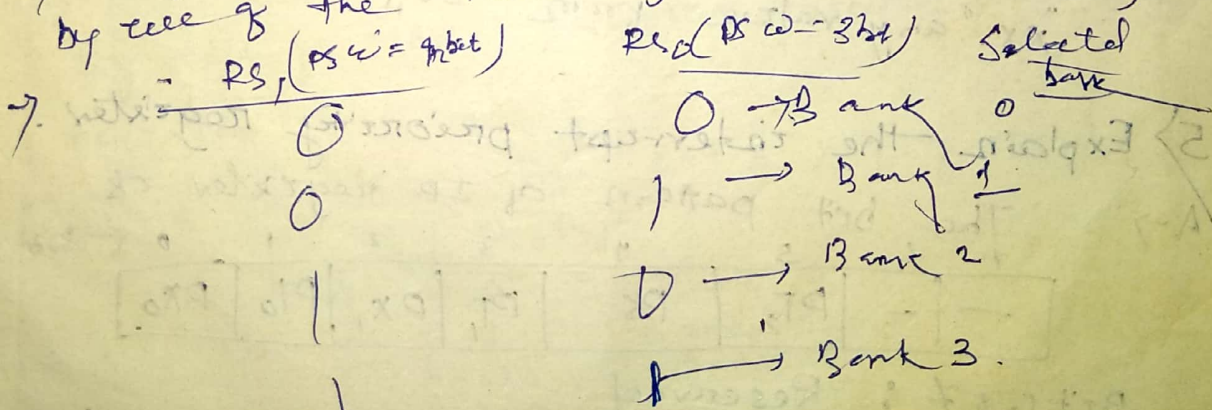
→ The DPTR doesnot have a single internal address but it has been allotted two addresses in the special function register bank for its two bytes DPH (83H) & DPL (82H)



Q.2) How to switch register banks in 8051?

A → When 8051 is powered on, register bank 0 is selected by default.

→ So it can be switched to other banks by use of the PSW registers (as bit 3 & 4 = 0)



→ These instructions can be "SETB" and "CLR"

3) What is 'LOOP' & nested loop?

A → LOOP is the repeating a sequence of instructions at a certain time is called a Loop.

→ In 8081 the loop action is performed by DJNZ reg. label.

→ A loop can be repeated a maximum of 255 times if register is FFH.

→ Nested LOOP is an action more times than 256 i.e. loop inside a loop.

→ So, multiple registers is used to hold the count.

4) What is the upper limit of the stack?

A → Locations 08H to 1FH in 8081 is

the RAM location is used for stack because 20H - 2FH of RAM is for bit addressable.

→ If the program more than 24 bytes of stack is needed then SP is changed to RAM location 30H - 7FH by the instruction "MOV SP, #XX" where "XX" any value from 30H to 7FH.

5) Explain the interrupt priority register.

A → The bit pattern of IP register is

7	6	5	4	3	2	1	0	Bit
—	—	PT ₂	PS	PT ₁	PX ₁	PT ₀	PX ₀	

Bit 6 & 7 : Reserved.

Bit 5 (PT₂) : Timer 2 interrupt priority (bit 8052 only).

Bit 4 (PS) : Serial Port interrupt priority bit.

Bit 3 (PT₁) : Timer 1 interrupt priority bit.

- Bit 2 (PX₁) :- External interrupt 1 priority bit.
 Bit 1 (PT₀) :- Timer 0 interrupt priority bit.
 Bit 0 (PX₀) :- External interrupt 0 priority bit.
 Priority bit = 1, assigns high priority.
 Priority bit = 0, assigns low priority.

6) Distinguish between 8051, 8052 and 8031 microcontrollers.

Feature	8051	8052	8031
(i) ROM (On chip program space in bytes)	4K	8K	0K
(ii) RAM (bytes)	128	256	128
(iii) Timers	2	3	2
(iv) I/O pins	32	32	32
(v) Serial port	1	1	1
(vi) Interrupt Sources	6	8	6

~~Repeat~~ How to switch register banks in 8051?
 when the 8051 is powered up, register bank 0 is selected by default.
 A → So, we can switch to other banks by using the program status word (PSW) register.
 bit 3, 4, 5, 6, 7 of PSW is done by

→ This is done by

PS ₁ (4)	PS ₀ (3)	
0	0	→ Bank 0
0	1	→ Bank 1
1	0	→ Bank 2
1	1	→ Bank 3

7) How stacks are accessed in 8051?

A → Stack is a selection of RAM used by CPU to store information temporarily.

→ The register used to access the stack is called the SP (Stack pointer) registers.

→ The SP is only 8 bits i.e. 00H to FFH.

→ When 8051 is powered up, the SP contains value 07H.

→ The stack operation is performed by "PUSH" and "POP" instructions.

8) Explain how a subroutine is executed with CALL instruction in the 8051?

A → (i) When a subroutine is called, control is transferred to that subrtn of the processor.

(ii) The address of the instruction immediately below the CALL is saved on the stack.

(iii) It fetches the instructions from the new address location (i.e. subroutines).

(iv) Then, the instruction RET is used to transfer the control back to main program or to the caller.

9) What are the external hardware interrupt of 8051 and how they triggered?

A → The 8051 has two external hardware interrupts.

→ Pin 12 (P3.2) and pin 13 (P3.3) of 8051 designated as INT0 and INT1 are used as external hardware interrupts.

INT0 → vector address (000BH)
INT1 → " " (001BH)

→ They are triggered by —

- (i) Level triggered
- (ii) Edge triggered.

10) What is addressing mode? How many types are there in 8051?

A → It is a technique which specifies the data in an instruction so that the CPU can access data in various ways.

→ 5 Addressing modes: —

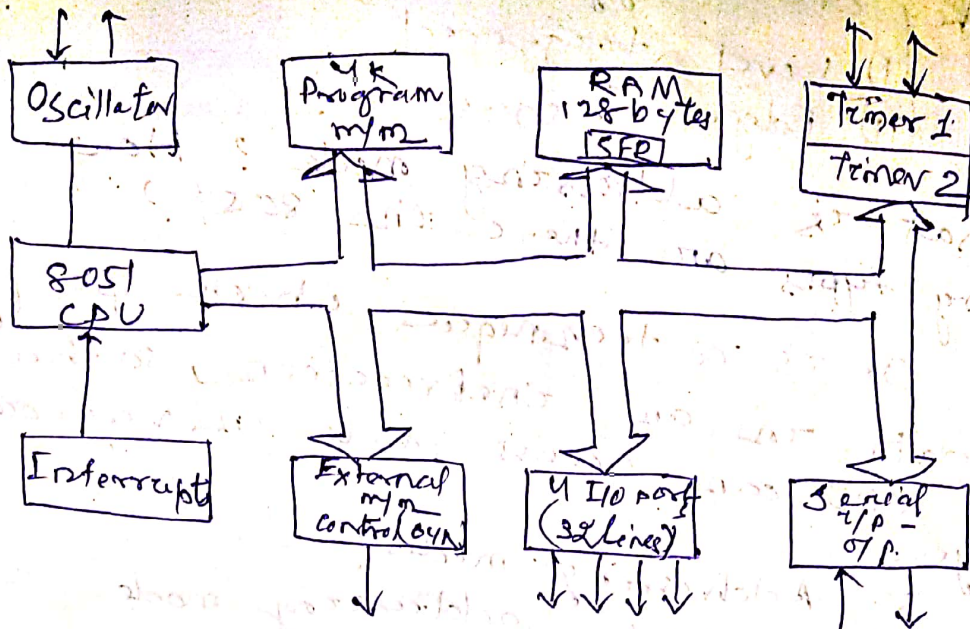
- (i) Immediate addressing mode
- (ii) Register
- (iii) Direct
- (iv) Register indirect
- (v) Indexed

Long type :-
Q.1) Write the features of 8051 microcontroller and also draw its simplified block diagram.

A → The features are: —

- (i) The 8051 is an 8-bit microcontroller.
- (ii) 4K (4096) bytes of on-chip ROM.
- (iii) 128 bytes of on-chip RAM (Data memory).
- (iv) Two timers, one serial port and four ports (each of 8 bit) available on a single chip.
- (v) The 8051 microcontroller has four register banks i.e. Bank 0, Bank 1, Bank 2, Bank 3.
- (vi) Two multiple mode, 16-bit timer/counter.
- (vii) One microsecond instruction cycle with 12 MHz crystal frequency.
- (viii) Direct Byte and bit addressability.
- (ix) Available with 40-pin DIP and DIP.

② Block diagram



2) Draw the bit pattern of program Status Word (PSW) of 8051 and explain the significance of each bit.

A → PSW —

→ Many instructions affect several status flags, which are grouped together to form the ~~PSW~~ PSW.

→ The bit pattern of the PSW is shown below.

→ PSW is a 8-bit word as —

7	6	5	4	3	2	1	0 Bit
CY	AC	FO	RS ₁	RS ₀	OV	-	P

Description —

→ Bit 0 → parity bit (P) — Set to 1 for even parity and 0 for odd parity.

→ Bit 1 — Reserved for future expansion

→ Bit 2 — Overflow flag (OV) — Set to 1 if the destination length is less than source length.

→ Bit-3, 4 — (RS_1, RS_0) — ^{For} Selecting the working register banks.

RS_1	RS_0	Bank selected
0	0	00H — 07H Bank 0
0	1	08H — 0FH Bank 1
1	0	10H — 17H Bank 2
1	1	18H — 1FH Bank 3

→ By default Bank-0 is selected when 8051 is powered on.

→ Bit-5 — User defined flag (F0) (flag zero)

→ Bit-6 — Auxiliary carry flag (AC), for BCD operations (i.e. carry at bit 3)

→ Bit-7 — Carry flag (CY) set if there is a carry from Bit-6, otherwise 0.

3) Write an assembly language program to perform multiplication of two 8-bit numbers using 8051 instructions set whose starting address is 4100H and two data are 80H and 80H. place their result at locations 4500H and 4501H.

```

A7      ORG      4100H      ; clear carry
        CLR      C
        MOV      A, #80H    ; Send 80H to ACC
        MOV      B, #80H    ; Send 80H to B register
        MOV      AB
        MUL      DPTR, #4500H
        MOV      @DPTR, A
        MOVX     DPTR
        INC      A, B
        MOV      @DPTR, A
        MOVX     HERE
        SJMP     HERE

```

4) Write a program to write the value 55H to RAM locations 40H-4FH and all these RAM locations contents together and save the result in RAM locations 60H and 61H in 8051.

A →

```
MOV A, # 55H
MOV R0, # 40H
MOV R2, # 05H
AGAIN: MOV @R0, A
      CLR A
      MOV 61H, A
      ADD A, @R0
      JNC NEXT
NEXT:  INC 61H
      MOV 60H, A
      INC R0
      DJNZ R2, AGAIN
```

5) Explain the different steps in executing an interrupt.

- A → Upon activation of an interrupt, the microcontroller goes through the steps:-
1. It finishes the instruction it is executing and saves the address of the next instruction (PC) on the stack.
 2. It also saves the current states of all the interrupts internally (i.e. on stack).
 3. It jumps to a fixed location in memory called the interrupt vector table that holds the address of the ISR.
 4. The microcontroller gets the address of the ISR from the interrupt vector table and jumps to it.
- It starts to execute the interrupt service subroutine until it reaches

(9)

the last instruction of the subroutine which is RETI (return from interrupt).

5. Upon executing the RETI instruction the microcontroller returns to the place where it was interrupted.

→ First, it gets the program counter (PC) address from the stack by popping the top two bytes of the stack into the PC.

→ Then it starts to execute from that address.

6) Explain Bit-Addressable RAM and Byte-Addressable RAM.

A → The bit-addressable RAM locations are $20H$ to $2FH$.

→ These 16 bytes provide 128 bits RAM bit-addressability, as $16 \times 8 = 128$ bits.

→ The 1st byte of internal RAM location $20H$ has bit address 0 to $7H$.

→ The last byte $2FH$ has bit address $78H$ to $7FH$.

→ Internal RAM locations $20 - 2FH$ are both byte and bit addressable.

→ Bank Registers are from $00 - 1FH$.

→ The below diagram below shows the whole arrangement: —

Byte-Addressable Location.

Bit-Addressable Locations

General Purpose RAM								
7F	7F	7E	7D	7C	7B	7A	79	78
70	77	76	75	74	73	72	71	70
6F	6F	6E	6D	6C	6B	6A	69	68
60	67	66	65	64	63	62	61	60
5F	5F	5E	5D	5C	5B	5A	59	58
50	57	56	55	54	53	52	51	50
4F	4F	4E	4D	4C	4B	4A	49	48
40	47	46	45	44	43	42	41	40
3F	3F	3E	3D	3C	3B	3A	39	38
30	37	36	35	34	33	32	31	30
2F	2F	2E	2D	2C	2B	2A	29	28
20	27	26	25	24	23	22	21	20
1F	1F	1E	1D	1C	1B	1A	19	18
10	17	16	15	14	13	12	11	10
0F	0F	0E	0D	0C	0B	0A	09	08
00	07	06	05	04	03	02	01	00
Bank 3 (R ₀ -R ₇)								
18								
17								
Bank 2 (R ₀ -R ₇)								
10								
0F								
Bank 1 (R ₀ -R ₇)								
08								
07								
Bank 0 (R ₀ -R ₇)								
00								