LECTURE NOTES

SUBJECT-BETC(1ST YEAR)

BRANCH-ALL

Department

of

Electronics and Telecommunication

Subject - BETC (Basic Electronics)
Semester - 1st

Semiconductor

Atomic Structure :-

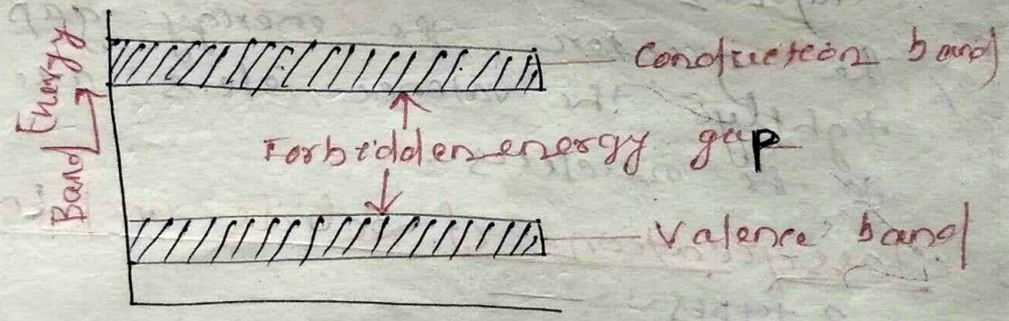
→ According to the modern theory, all the materials are composed of very small particles called atom.

→ An atom consists of a central nucleus of positive charge around which small negatively charged particles called electrons revolves in different circular orbits or paths.

→ The electrons in each permitted orbit have a certain fixed amount of energy. The larger the orbit (i.e. largest radius) the greater is the energy of electrons (ele.).

Energy Band :-

Definition :- The range of energies possessed by an ele. in a solid is known as energy band.



Valence band :-

→ The range of energies (i.e. band) possessed by valence electrons is known as valence band.

→ The ele.s in the outermost orbit of an atom are known as valence electrons.

→ In a normal atom, valence electrons have highest energy.

→ This band may be completely or partially filled.

For ex :- Inert gases have full completely filled valence band.

Conduction band :—

def^n :- The range of energies (i.e. band) possessed by conduction band electrons is known as conduction band.

→ The valence electrons are loosely attached to the nucleus. These ele.s may get detached to become free electrons and these free ele.s are responsible for current conduction.

→ For this reason, they are called conduction ele.s.

→ So, insulators have empty conduction band but conductors have partially filled conduction band.

Forbidden energy gap :—

def^n :- The separation between conduction band and valence band on the energy band diagram is known as forbidden energy gap.

→ The greater the energy gap, more tightly the valence ele.s are bound to the nucleus.

Classification of Solids and Energy bands:

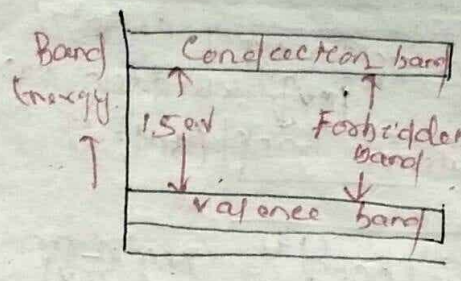
3 types :—

1. Insulator
2. Conductor
3. Semiconductor.

(1) Insulator :—

→ Insulators are those substances which do not allow the passage of electric current through them.

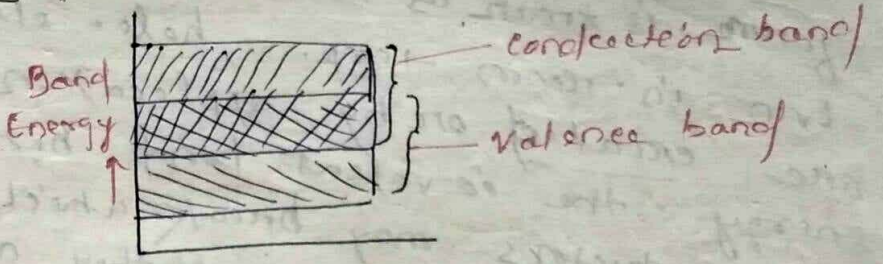
→ In terms of energy band, the valence band is full while the conduction band is empty.



→ the energy gap between valence and conduction band is very large (≃15eV).
→ So, a very high electric field is required to push the valence e/e.s. to the conduction band.

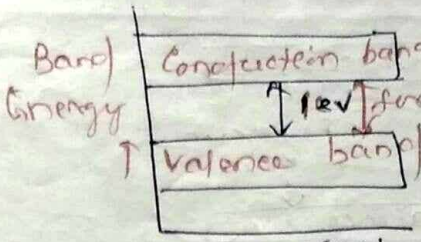
Ex:- Wood, glass etc.

② Conductors :-
→ Conductors are those substances which easily allow the passage of electric current through them.
→ In terms of energy band, the valence and conduction bands overlap each other and therefore a large no. of free electrons are available.



Ex:- Copper, Aluminium.

③ Semiconductor :-
→ Semiconductor are those substances whose electrical conductivity lies inbetween conductors and insulators.
→ In terms of energy band, the valence band is almost filled and conduction band is almost empty.
→ The energy gap is very small i.e. electric field required is smaller than insulators but much greater than conductors.



Ex:- Carbon, Silicon (14) (1.1ev), Germanium (32) (0.7ev), Selenium etc.

→ In other word, a semiconductor is a substance which has resistivity (10^{-4} to 0.5Ωm) inbetween conductors & insulators.

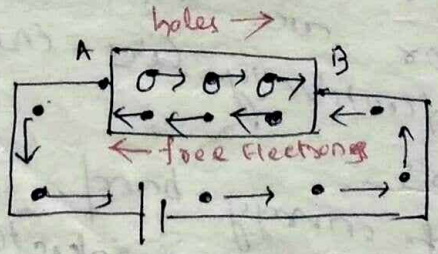
→ Semiconductors have negative temperature co-efficient of resistance. i.e. the resistance value decreases with the increase in temp. and vice versa.

→ Semiconductor is 2 types :-
1. Intrinsic Semiconductor
2. Extrinsic Semiconductor

Intrinsic semiconductor :-

→ A semiconductor in an extremely pure form is known as intrinsic semiconductor.

→ Even in room temp. hole-electron pairs are created or by application of external energy the co-valent bond between the semiconductor's may break which produces hole-electron pair and they are responsible for current conduction.



* Hole :- When a valence electron leaves the valence band & enters into the conduction band, then a hole is created in the valence band.

→ So, a hole is a positively charge particle and current due to hole is called as hole current.

Extrinsic Semiconductor :-

→ To increase the conducting properties of the pure semiconductor, a small amount of suitable impurity is added to that semiconductor. It is then called impure or extrinsic semiconductor.

→ So, the process of adding impurities to a semiconductor is known as doping.

→ Extrinsic semiconductors is two types :-

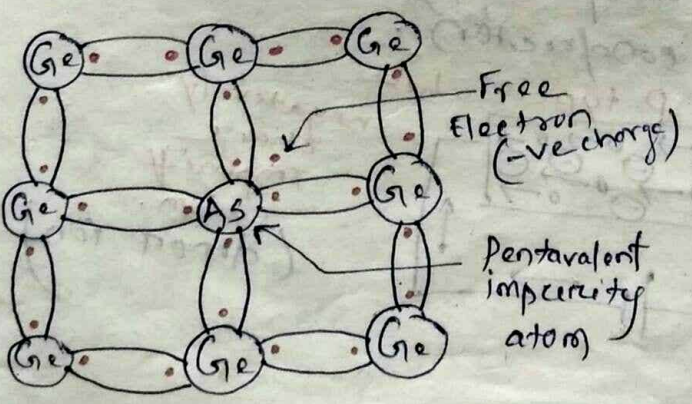
1. N-type semiconductor.
2. P-type semiconductor.

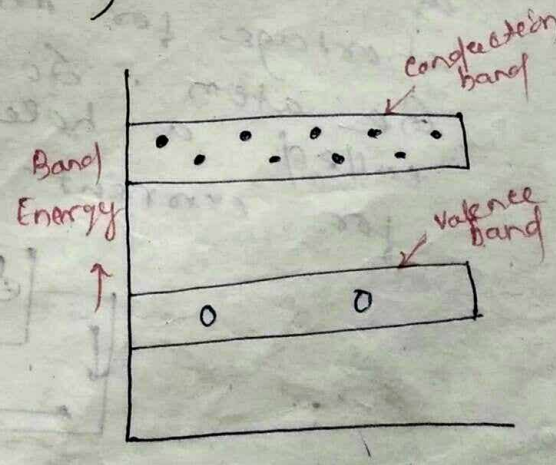
N-type Semiconductor :-

→ When a small amount of pentaval ent impurity (having 5 valence ele.s) is added to a pure semiconductor, it is known as N-type semiconductor.

→ Examples of pentavalent impurities are Arsenic (As) (33) and Antimony (Sb) (51).

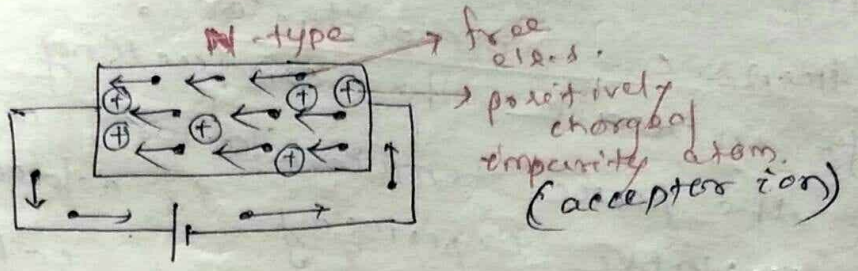
→ Such impurities which produces n-type semiconductor are known as donor impurity because they donate or provide free ele.s to the semiconductor crystal.





(Energy Band diagram of N-type)

→ So, in this case no. of free ele.s are more & they are responsible for current conduction.

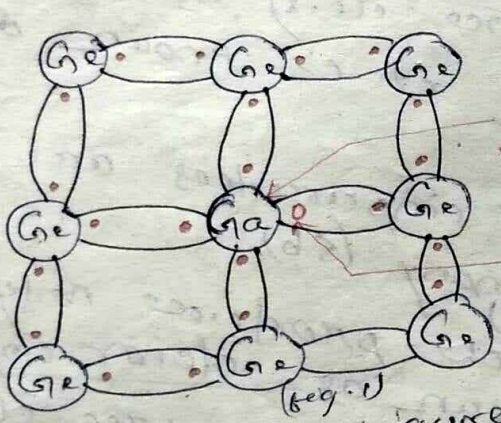


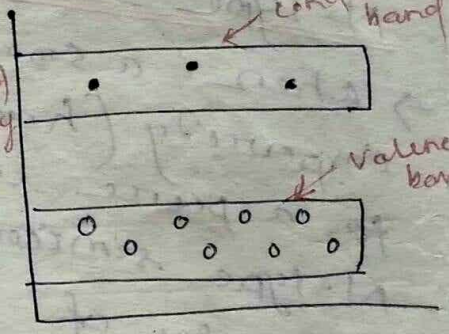
P-type Semiconductor :—

→ When a small amount of trivalent impurity (3 valence ele.s) is added to a pure semiconductor, it is called P-type semiconductor.

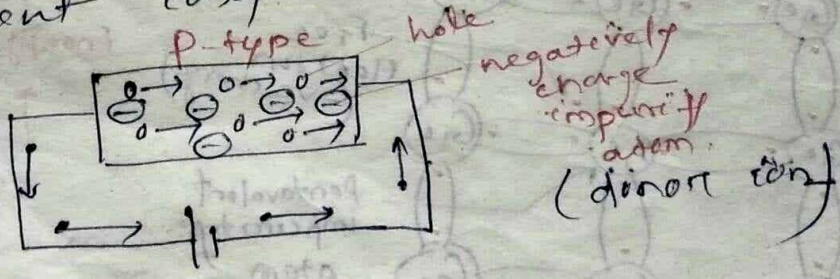
→ Examples of trivalent impurities are Gallium (Ga) (31) and Indium (In) (49).

→ Such impurities which produce P-type semiconductor are known as acceptor impurities because the holes created can accept the electrons.





→ From the figure i, it is clear that as Ga has 3 valence ele.s, one ele. is shortage for making covalent bond with Ge atom. So this missing of ele. is called a hole and they are responsible for current conduction.



Majority and Minority Carriers :-

→ The carriers which plays a majority portion of current flow are known as majority carriers and that have less responsibility in current conduction are known as minority carriers.

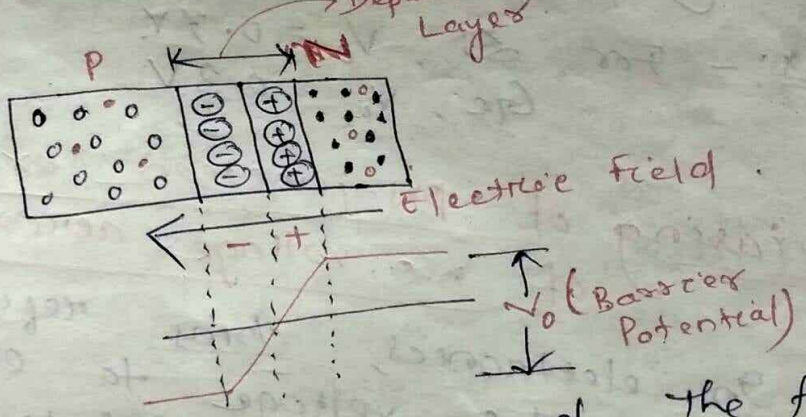
→ For N-type, free ele.s → majority carriers
holes → minority carriers.

→ For P-type, holes → majority carriers,
Electrons → minority carriers.

PN Junction :-

→ When a P-type semiconductor is suitably joined to N-type semiconductor, the contact surface is called PN-junction.

Properties of PN-junction :-



→ When PN-junction is formed, the free-ele.s near the junction in the n-region begin to diffuse into the P-region where they combine with holes near the junction. So, n-region loses free ele.s & create a layer of positive charges.

→ Similarly, in the p-region, as the ele.s move across the junction, it loses holes as ele.-hole combine & create a layer of negative charges.

→ These two layers of positive and negative charges form the depletion region or depletion layer. This means near the junction, the region is depleted (i.e. emptied) of charge carriers (free e/e.s and holes).

→ Once PN-junction is formed and depletion layer is created, the diffusion of free-e/e.s stop. In other words, depletion region acts as a barrier to further movement.

→ The +ve & -ve charge set up an electric field and a potential difference is generated across the depletion layer which is called as potential barrier (V_0).

→ The potential barrier depends on:—
1. Type of semiconductor material
2. Amount of doping
3. Temperature.

Ex:- For Si, $V_0 = 0.7V$
Ge, $V_0 = 0.3V$

Biasing of PN-junction or Application of D.C. voltage across PN-junction:

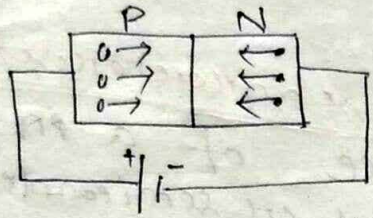
→ In electronics, bias refers to the use of d.c. voltage to establish certain operating conditions for an electronic device.

→ There two bias condition is present.
1. Forward biasing
2. Reverse biasing.

① Forward Biasing :-

→ when external d.c. voltage applied to the junction in such a direction that it cancels the potential barrier and permitting current flow it is called forward biasing.

→ In this case, the +ve terminal of the battery is connected to P-type and -ve terminal is connected to N-type as shown in figure.



→ Due to application of external forward potential, the barrier voltage or potential barrier is gradually reduced and at some potential, it is eliminated.

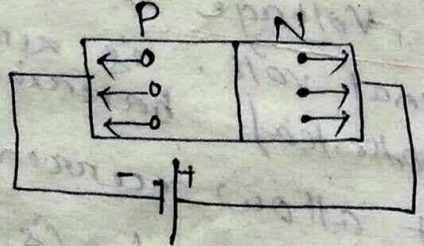
→ So, the junction offers low resistance (called forward resistance, R_f) to current flow.

→ The magnitude of current depends upon the applied forward voltage.

② Reverse Biasing :-

→ When the external d.c. voltage applied to the junction is in such a direction that potential barrier is increased, it is called reverse biasing.

→ In this case, the -ve terminal of the battery is connected to P-type and +ve terminal is connected to N-type as shown in figure.



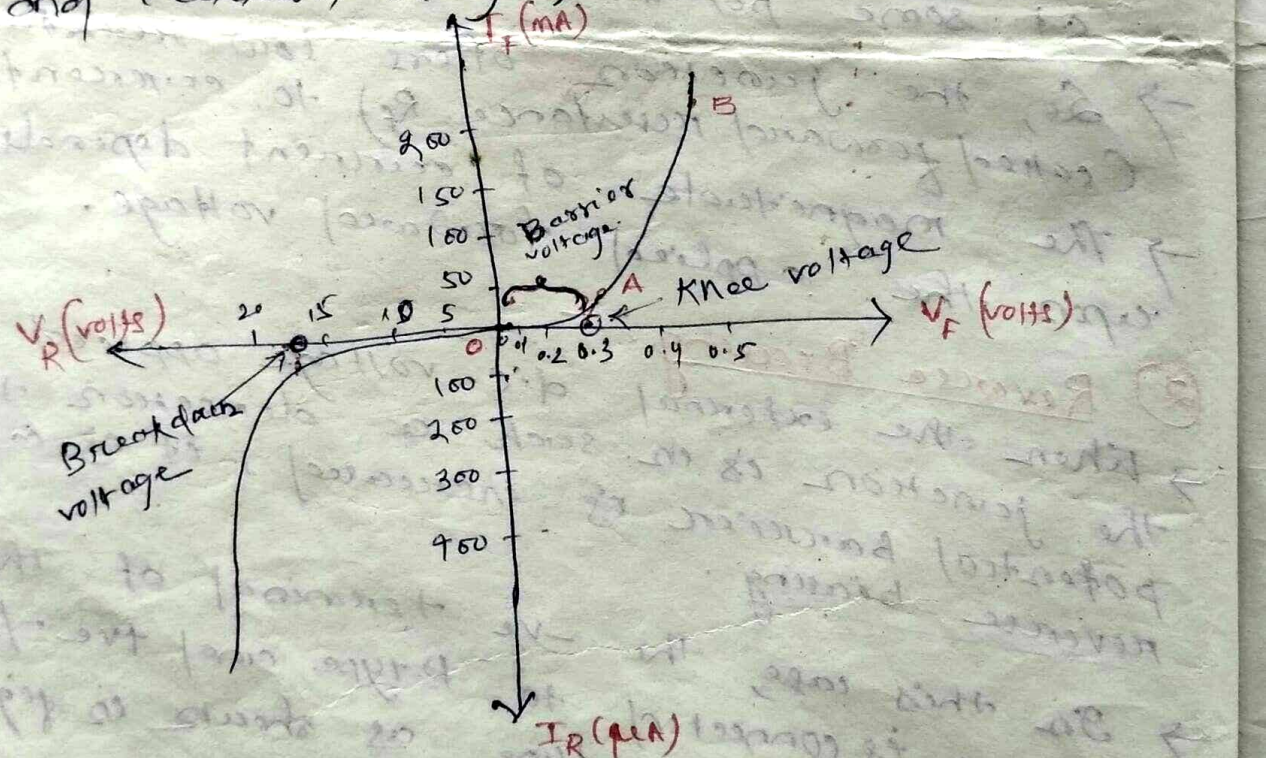
→ Due to the reverse voltage, it strengthens the electric field of the barrier potential is increased which prevents the flow of charge carriers across the junction.

→ Thus, a high resistance path is established and hence the current does not flow. This resistance is called as Reverse resistance, R_R.

Volt-Ampere (V-I) characteristics of PN-junction

→ V-I characteristics of a PN junction (also called crystal or semiconductor diode) is the curve between voltage across the junction and the circuit current.

→ Here, voltage is taken along x-axis and current along y-axis.



(i) Zero External Voltage :-

→ When the external volt. is zero i.e. circuit is open, the potential barrier at the junction does not allow current flow.

→ So, the circuit current is zero as indicated by point 0.

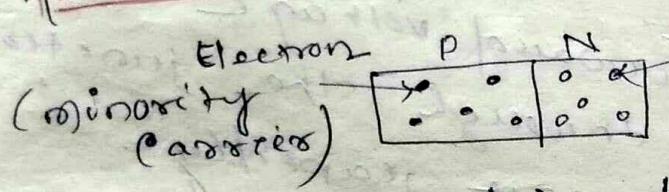
(ii) Forward Bias :—

→ With forward bias the P-type connected to +ve terminal and N-type connected to -ve terminal, the potential barrier is reduced.

→ At some forward volt. (0.7V for Si & 0.3V for Ge) the potential barrier is eliminated & current starts flowing.

→ It is shown in the region OA at first i.e. the current increases very slowly & the curve is non-linear (AB)

(iii) Reverse Bias :—



→ With reverse bias to the PN-junction P-type is connected to -ve & N-type is connected to +ve terminal, the barrier potential is increased & no current flows practically.

→ However, a very small current (order of μA) flows called as reverse saturation current (I_s) and is due to the minority carriers.

→ If reverse volt. is increased continuously, the KE (Kinetic Energy) of electrons (minority carriers) become high enough to knock out ele.s from semiconductor atoms.

→ At this stage breakdown of the junction occurs, so that sudden rise of reverse current occurs.

→ So, the voltage at which PN junction breaks down with sudden rise in reverse current is known as breakdown voltage.

→ Important terms:

(1) Breakdown voltage — (Zener voltage)

→ It is the minimum reverse voltage at which PN-junction breaks down with sudden rise in reverse current.

→ Due to increase in reverse voltage, the newly liberated ele.s in term free other valence ele.s. In this way, we get an avalanche of free ele.s and this point is known as avalanche breakdown.

→ Thus, PN-junction conducts a very large reverse current.

(11) Knee voltage :—

→ It is the forward voltage at which the current through the junction starts to increase rapidly.

(111) Peak inverse voltage :—

→ It is the maximum reverse voltage that can be applied to the PN-junction without damage to the junction.

Zener Diode :—

→ A properly doped crystal diode which has a sharp breakdown voltage is known as a zener diode.

→ During reverse bias of a crystal diode, the breakdown volt. is reached where the reverse current increases sharply.

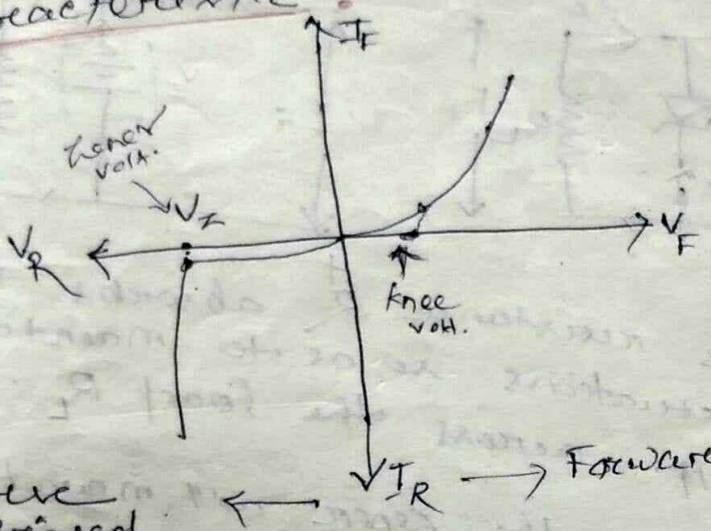
→ This breakdown was first given by the American scientist C. Zener.

→ Therefore, the breakdown volt. is sometimes called Zener voltage and the current is called Zener current.

→ The zener volt. depends upon the amount of doping.

→ If the diode is heavily doped, depletion layer will be thin and breakdown will occur at a lower reverse volt.

characteristic :—



Reverse Biased characteristic ← → Forward Biased characteristic

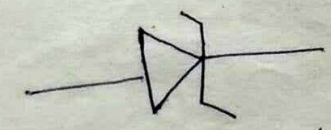
→ A zener diode is like an ordinary diode except that it is properly doped so as to have a sharp breakdown voltage called as zener volt. V_Z.

→ A zener diode is always reverse connected i.e. it is always reverse biased.

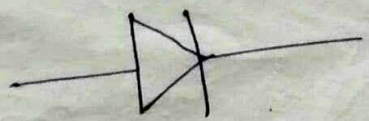
→ When forward biased, its characteristics are just those of ordinary diode.

→ The zener diode is not immediately burnt just because it has entered the breakdown region.

Symbol :—



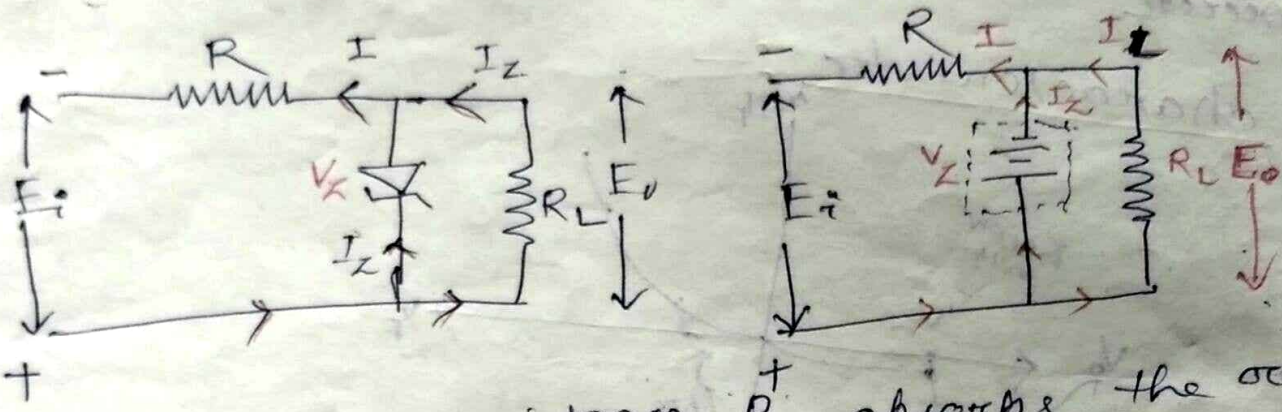
(Zener diode)



(Crystal diode / Diode)
PN-junction diode

Zener Diode as Voltage Stabilizer :-

→ A Zener diode can be used as a volt. regulator to provide a constant volt. from a source whose volt. may vary over sufficient range.



→ The series resistance R absorbs the output voltage fluctuations so as to maintain constant volt. across the load R_L.

→ In this case, the Zener will maintain a constant volt. $V_Z (= E_o)$ across the load as long as the input volt. doesn't fall below V_Z.

Now, Volt. drop across $R = E_i - E_o$

Current through R, $I = I_Z + I_L$

Applying ohm's law, we have

$$R = \frac{E_i - E_o}{I_Z + I_L}$$

This is also the impedance of zener diode.

Rectifier:

→ A rectifier is a circuit, which uses one or more diodes to convert a.c voltage into pulsating d.c voltage.

→ The rectification is the process in which the a.c input is convert into d.c output.

→ The rectifier is of two types:

(a) Half-wave rectifier

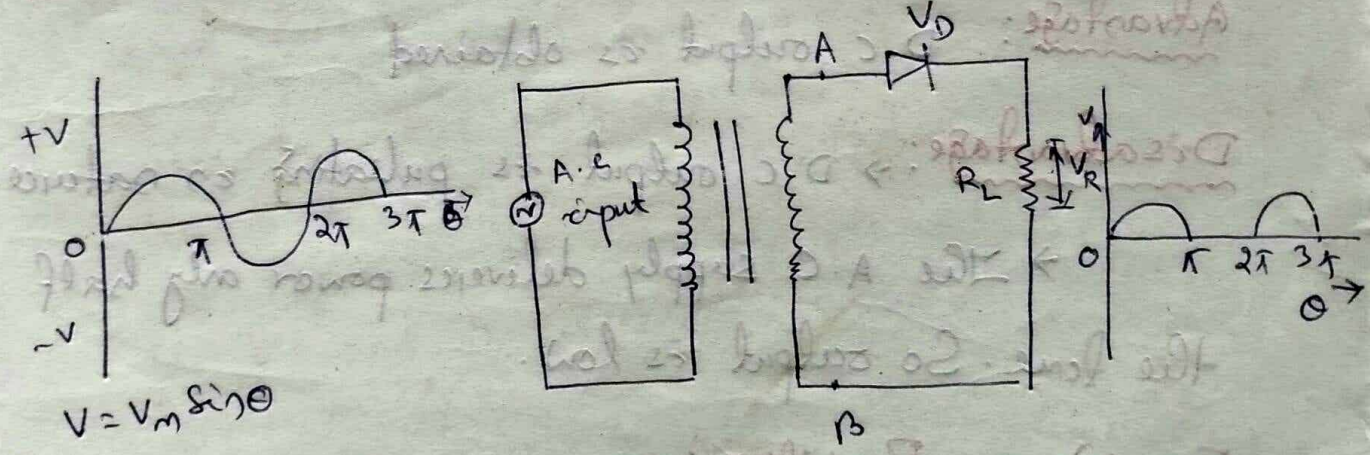
(b) Full-wave rectifier

→ The full wave rectifier is of two types.

ⓐ Centre-tapped full wave rectifier

ⓑ Bridge type full wave rectifier.

Half-wave rectifier:



→ These are the circuit where half of the Ac input is rectified.

→ We will have the voltage across the positive half cycle only.

→ In half wave rectifier a single crystal diode is used across the secondary winding.

→ Let for the 1st +ve half cycle, the point A is +ve w.r.t point B.

→ In this condition the diode is forward biased and direction shown in the figure.

→ In the 1st -ve half cycle the point A is -ve w.r.t point B.

→ In this condition diode is reversed biased and the circuit is a open circuit for which no conduction takes place across the diode and there is no output voltage across the load resistance.

→ The current across the output flows only in one direction is from point A to point B.

Advantage: D.C output is obtained

Disadvantage: → D.C output is pulsating in nature.

→ The A.C supply delivers power only half the time. So output is low.

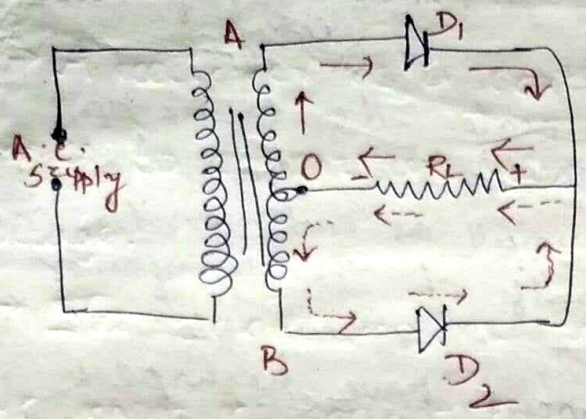
Full Wave Rectifier :—

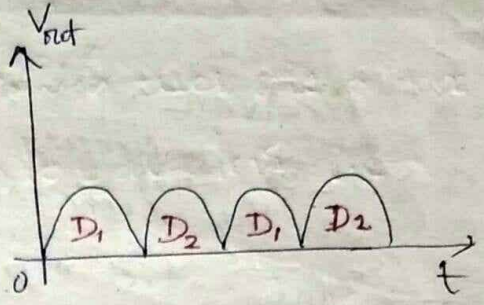
→ In fullwave rectification, current flows through the load in the same direction for both half-cycles of i/p a.c. voltage.

→ Two types —

① Centre tap F.W.R
② Full wave bridge rectifier

Centre-tap FullWave Rectifier:-





→ The circuit consists of two diodes D_1 & D_2 as shown in figure.

→ A centre tapped secondary winding AB is used in which two diodes D_1 & D_2 are connected.

Operation:—

→ During +ve half cycle of secondary voltage, the end A of the secondary winding becomes +ve and end B becomes -ve. This makes the diode D_1 forward biased and diode D_2 reverse biased i.e. D_1 conducts while D_2 does not conduct.

→ The current then flow through D_1, Load resistor R_L and the upper half of secondary winding as indicated ~~line~~ arrows.

→ During -ve half cycle, the end A becomes -ve and end B becomes +ve.

→ Therefore, D_2 conducts as it is forward biased and D_1 doesnot conducts as it is reverse biased.

→ So, the current flows through D_2, load R_L and lower half winding as shown by dotted arrows.

→ It is seen that current flows in the load R_L is in the same direction for both half cycles.

→ Therefore, d.c. is obtained across load R_L.

Peak Inverse Voltage :—

$PIV = 2V_m$ V_m = maximum volt. across the half secondary winding.

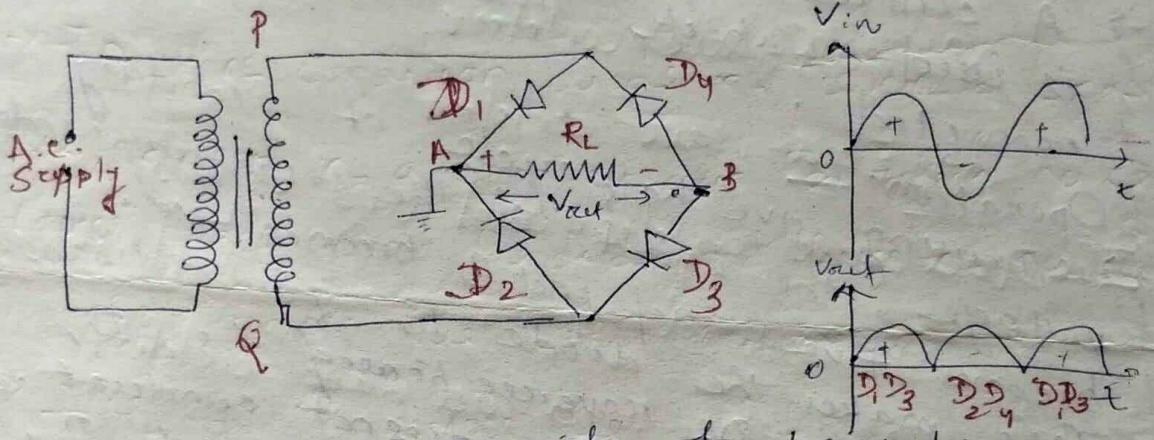
Disadvantages :—

→ It is difficult to locate the centre tap on the secondary winding.

→ The d.c. o/p is small as each diode utilises only on half of the transformer secondary voltage.

→ The diodes used must have high peak inverse voltage.

Full-Wave Bridge Rectifier :—



→ This rectifier consists of four diodes D_1, D_2, D_3 & D_4 which are connected to form bridge.

→ The a.c. supply to be rectified is applied to the diagonally opposite ends of the bridge through the transformer.

→ A load resistance R_L is connected across the other two ends of the bridge.

Operation :—

→ During the positive half cycle of secondary voltage, the end P is +ve and end Q is -ve.

→ This makes D_1 and D_3 forward biased while D_2 & D_4 are reverse biased.

→ Therefore, only diodes D_1 & D_3 conduct then, the current flows across the load R_L from A to B.

→ During -ve half cycle of secondary voltage, end P becomes -ve and end Q, +ve which makes D_2 and D_3 are forward biased and D_1, D_3 are reverse biased.

→ Therefore only D_2 & D_4 conduct and D_1 & D_3 doesnot conducts.

→ Then the current flow through load R_L from A to B i.e. in the same direction as for +ve half-cycle.

→ Hence, d.c. output is obtained across load R_L.

Peak inverse voltage — PIV of each diode is equal to the maximum voltage (V_m) across the secondary.

Advantages: —

→ The need for centre-tapped transformer is eliminated.

→ The o/p is twice that of the centre-tap circuit for the same secondary voltage.

→ The PIV is one-half that of the centre-tap ckt (for same d.c. o/p).

Disadvantages: —

→ It requires four diodes.

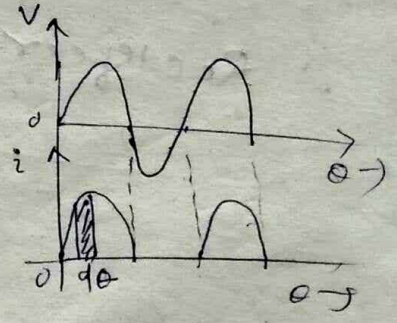
→ Voltage drop in the internal resistance of the rectifying circuit.

Efficiency —

Half Wave Rectifier :—

→ The ratio of d.c. power o/p to the applied i/p a.c. power is known as rectifier efficiency

i.e. $$\eta = \frac{\text{d.c. power output}}{\text{a.c. power input}}$$



Let $v = V_m \sin\theta$ be the alternating volt. that appears across the secondary winding.

Let r_f = diode resistance

R_L = load resistance.

d.c. power :—

The o/p current is pulsating dc. So, in order to find d.c. power, average current has to be found out.

$$I_{av} = I_{dc} = \frac{1}{2\pi}\int_0^{\pi} i\,d\theta = \frac{1}{2\pi}\int_0^{\pi} \frac{V_m \sin\theta}{r_f + R_L}\,d\theta.$$

$$\left[\because \text{Avg. value} = \frac{\text{Area under the curve}}{\text{Base}} = \frac{\int_0^{\pi} i\,d\theta}{2\pi}\right]$$

$$\Rightarrow I_{dc} = \frac{V_m}{2\pi(r_f + R_L)}\int_0^{\pi} \sin\theta\,d\theta$$

$$= \frac{V_m}{2\pi(r_f + R_L)}\left[-\cos\theta\right]_0^{\pi} = \frac{V_m}{2\pi(r_f + R_L)} \times 2$$

$$= \frac{V_m}{(r_f + R_L)} \times \frac{1}{\pi}$$

$$= \frac{I_m}{\pi} \qquad \left[\because I_m = \frac{V_m}{(r_f + R_L)}\right]$$

$\therefore$ d.c. power, $P_{dc} = I_{dc}^2 \times R_L = \left(\frac{I_m}{\pi}\right)^2 \times R_L$.

a.c. power input :—

$$P_{a.c} = I_{rms}^2 (r_f + R_L)$$

For half wave rectifier, $I_{rms} = I_m/2$

$$P_{ac} = \left(\frac{I_m}{2}\right)^2 \times (r_f + R_L)$$

Rectifier efficiency $= \dfrac{\text{d.c. o/p power}}{\text{a.c. i/p power}}$

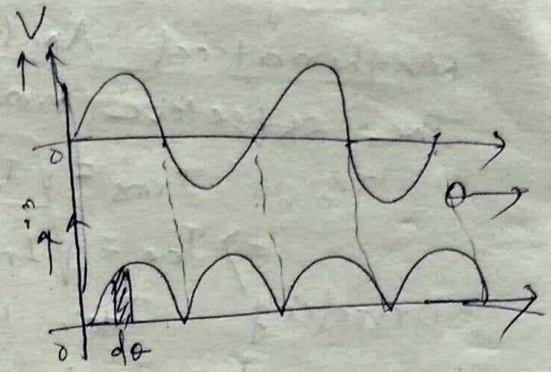
$$= \frac{(I_m/\pi)^2 \times R_L}{(I_m/2)^2 \times (r_f + R_L)}$$

$$= \frac{0.406\,R_L}{r_f + R_L} \Rightarrow \boxed{\frac{0.406}{1 + \frac{r_f}{R_L}} = \eta}$$

If r_f is negligible

$\therefore$ Max. rectifier efficiency = 40.6 %

Full Wave Rectifier :-



→ Let $V = V_m \sin\theta$ be the a.c. voltage to be rectified.

→ r_f & R_L be the diode resistance & load resistance.

Now, instantaneous current

$$i = \frac{V}{r_f + R_L} = \frac{V_m \sin\theta}{r_f + R_L}$$

d.c. output power :- the o/p is pulsating d.c.

So the dc power is average current i.e.

$$I_{dc} = \frac{1}{\pi}\int_0^{\pi} i \cdot d\theta =$$

$$\Rightarrow I_{dc} = \frac{2I_m}{\pi}$$

$\therefore$ d.c. power o/p, $P_{dc} = I_{dc}^2 \times R_L = \left(\frac{2I_m}{\pi}\right)^2 \times R_L$

a.c. input power :-

$$P_{ac} = I_{rms}^2 (r_f + R_L)$$

For a full wave rectifier, $I_{rms} = I_m/\sqrt{2}$

$$\therefore P_{a.c.} = \left(\frac{I_m}{\sqrt{2}}\right)^2 (r_f + R_L)$$

$\therefore$ Full wave rectification efficiency is

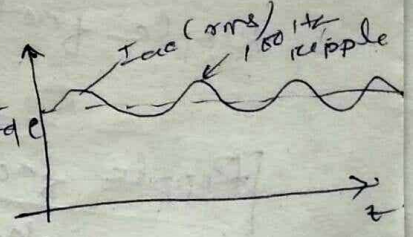
$$\eta = \frac{P_{dc}}{P_{ac}} = \frac{(2I_m/\pi)^2 \cdot R_L}{\left(\frac{I_m}{\sqrt{2}}\right)^2 (r_f + R_L)}$$

$$= \frac{8}{\pi^2} \times \frac{R_L}{(r_f + R_L)} = \frac{0.812 R_L}{r_f + R_L} \Rightarrow \boxed{\frac{0.812}{1 + \frac{r_f}{R_L}} = \eta}$$

If r_f is negligible as compared to R_L then

Maximum efficiency = 81.2%.

Ripple Factor :-



→ The o/p of a rectifier consists of a d.c. component and an a.c. component (also known as ripple).

→ The ratio of r.m.s. value of a.c. component to the d.c. component in the rectifier is known as **ripple factor** i.e.

$$\text{Ripple factor} = \frac{\text{r.m.s. value of a.c. component}}{\text{value of d.c. component}} = \frac{I_{ac}}{I_{dc}}$$

→ The smaller the ripple factor, the lesser the effective a.c. component and hence more effective is the rectifier.

Mathematical Analysis :-

The effective (r.m.s) value of total load current is, $I_{rms} = \sqrt{I_{dc}^2 + I_{ac}^2}$

$$\Rightarrow I_{ac} = \sqrt{I_{rms}^2 - I_{dc}^2}$$

Dividing I_{dc}, we get,

$$\frac{I_{ac}}{I_{dc}} = \frac{1}{I_{dc}} \sqrt{I_{rms}^2 - I_{dc}^2}$$

But I_{ac}/I_{dc} is ripple factor,

$$\therefore \text{Ripple factor} = \frac{1}{I_{dc}} \sqrt{I_{rms}^2 - I_{dc}^2}$$

$$= \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$$

(1) For half-wave rectification :-

→ In half wave rectification

$I_{rms} = I_m/2$, $I_{dc} = I_m/\pi$

$$\therefore \text{Ripple factor} = \sqrt{\left(\frac{I_m/2}{I_m/\pi}\right)^2 - 1}$$

Ripple factor = 1.21

→ It is clear that a.c. exceeds d.c. component i.e. greater pulsation in the o/p. So halfwave is ineffective for a.c. to d.c. conversion.

(2) For FullWave rectification :-

In full wave

$I_{rms} = \frac{I_m}{\sqrt{2}}$, $I_{dc} = \frac{2I_m}{\pi}$

$$\text{Ripple factor} = \sqrt{\left(\frac{I_m/\sqrt{2}}{2I_m/\pi}\right)^2 - 1}$$

Ripple factor = 0.48

→ It is clear that d.c is more than a.c component. So, fullwave rectification is used for a.c. to d.c. conversion.

Comparasion :-

		HalfWave	Centretap	Bridge type
(1)	No. of diodes	1	2	4
(2)	Transformer necessary	no	yes	no
(3)	Max. efficiency	40.6%	81.2%	81.2%
(4)	Ripple factor	1.21	0.48	0.48
(5)	Output frequency	f_{in}	$2f_{in}$	$2f_{in}$
(6)	Peak inverse voltage (PIV)	V_m	$2V_m$	V_m

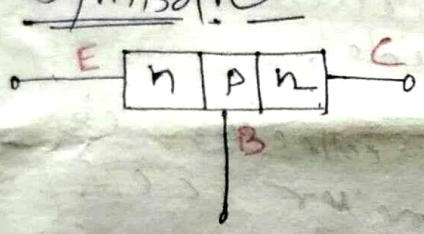
TRANSISTOR

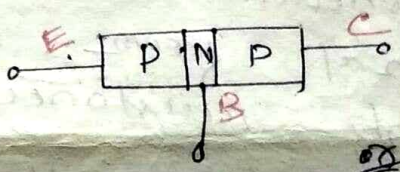
→ A transistor consists of two PN-junctions formed by sandwiching either P-type or n-type semiconductor between a pair of opposite types.

→ It is of two types –
1. n-p-n transistor
2. p-n-p transistor.

→ The transistor has three regions. (three terminals) namely :–
1. Emitter (E)
2. Base (B)
3. Collector (C)

Symbol :–





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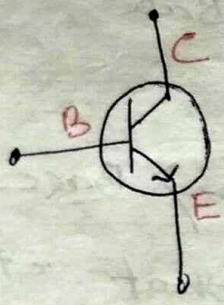

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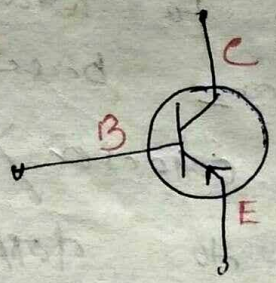


(i) Emitter :–
→ The section on one side that supplies charge carriers (electrons or holes) is called the emitter.
→ The emitter is always forward biased w.r.t. base, so that it can supply a large number of majority carriers.

(ii) Collector :–
→ The section on the other side that collects the charges is called the collector.

→ The collector is always reverse biased w.r.t. base.

(iii) Base :—

→ The middle section which forms two PN-junctions between the emitter and collector is called the base.

⇒ The base-emitter junction is forward biased that allows low resistance path.

⇒ Similarly, base-collector junction is reverse biased and provides high resistance path.

⇒ So, the name is transfer of resistor i.e. transistor or transfer of a signal from low resistance side to high resistance side.

⇒ According to wideness, collector is widest than base & emitter i.e.

wide → Collector > Emitter > Base.

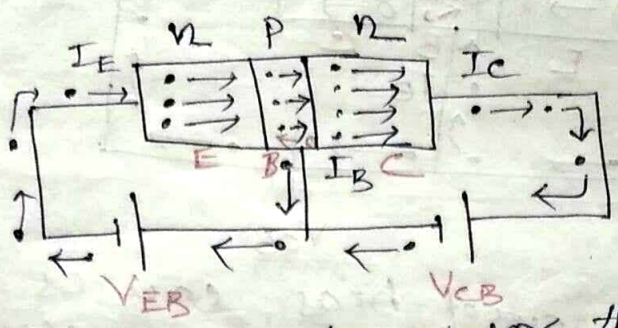
⇒ According to dopping,

Doping → Emitter > Collector > Base.

→ Emitter is heavily doped so that it can inject a large number of charge carriers (electrons or holes) into the base.

Working of transistor :-

npn transistor :-



→ In this npn transistor the E-B junction is forward biased and C-B junction is reverse biased.

→ This forward bias causes the electrons in the n-type emitter to flow towards the base which constitute emitter current I_E.

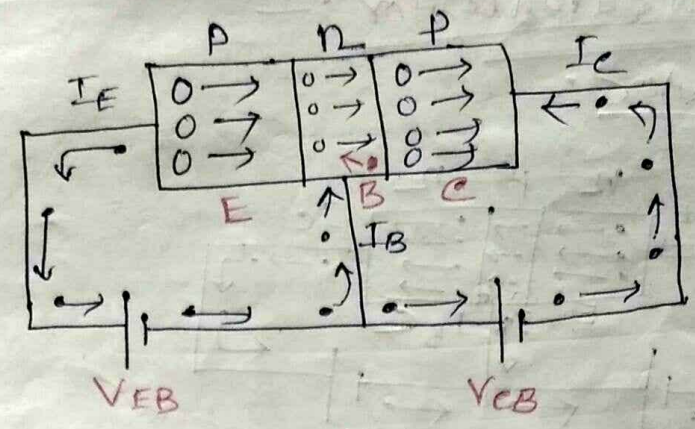
→ As the base is thin & lightly doped of P-type, some (very less no.) electrons combine with the holes & rest amount cross over to collector region which constitute base current I_B & collector current I_C respectively.

→ The reverse bias on collector is quite high and exerts attractive forces on these electrons & the I_C flows.

→ It is clear that emitter current is sum of collector & base current. i.e. $\boxed{I_E = I_B + I_C}$.

PNP transistor :-

→ In the PNP transistor the E-B junction is also forward biased and C-B junction is reverse biased.



→ The forward bias causes the holes in the p-type emitter to flow towards the base and that constitute emitter current I_E.

→ As base is thin & lightly doped less than 5%. holes combine with ele. in n-type & rest amount cross to collector region.

→ So, base current (I_B) and collector current (I_C) flow across the circuit.

→ It may be noted that current conduction in PNP transistor is by holes & $\boxed{I_E = I_C + I_B}$.

Transistor Connections / Configurations —

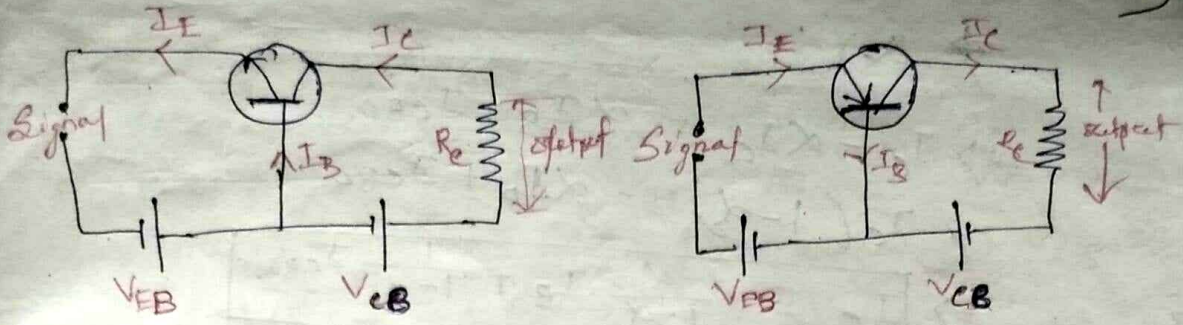
→ A transistor can be connected in a circuit in 3 ways :—

(i) Common base connection (CB)
(ii) Common emitter connection (CE)
(iii) Common collector connection (CC)

(i) Common base Connection :—

→ In CB connection input (i/p) is applied between E and B and output (o/p) is ~~applied~~ taken between C and B.

→ Here, base (B) is common to both i/p & o/p circuits (ckt) & hence the name CB connection



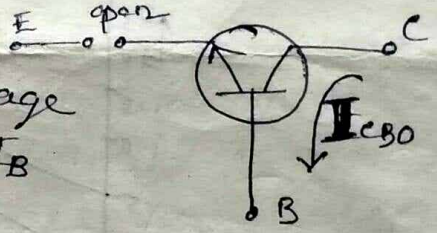
(1) Current amplification factor (α) :—

→ The ratio of change in collector current to the change in emitter current at constant collector base voltage V_{CB} is known as current amplification factor i.e.

$$\alpha = \frac{\Delta I_C}{\Delta I_E}, \text{ at constant } V_{CB}$$

(2) Expression for collector current :—

→ The whole emitter current does not reach to collector because a small percentage of it give rise to I_B due to electrone-hole combination in base area.



→ So, the total collector current consists of

(i) The part of emitter current which reaches to the collector terminal i.e. αI_E $\left(\because \alpha = \frac{I_C}{I_E} \Rightarrow I_C = \alpha I_E\right)$

(ii) The leakage current $I_{leakage}$. This is due to the movement of minority carriers across B-C junction being reverse biased.

Therefore, $I_C = \alpha I_E + I_{leakage}$

$\Rightarrow I_C = \alpha I_E + I_{CBO}$ [∵ when emitter is open i.e. $I_E = 0$, small current I_{CBO} is flowing]

Now, $I_E = I_C + I_B$

$\therefore I_C = \alpha(I_C + I_B) + I_{CBO}$

$\Rightarrow$ I_B ?

$\Rightarrow I_c - \alpha I_c = \alpha I_B + I_{CBO}$

$\Rightarrow I_c(1-\alpha) = \alpha I_B + I_{CBO}$

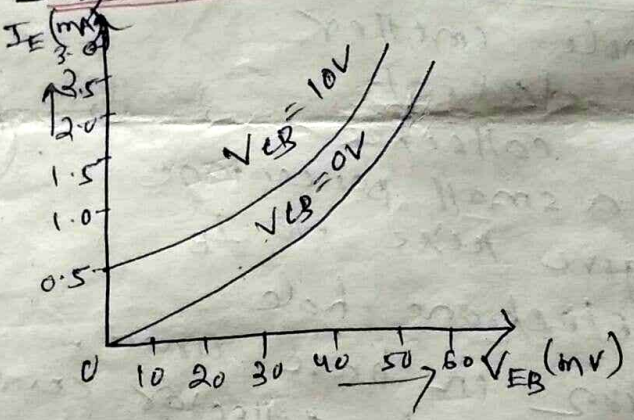
$\Rightarrow \boxed{I_c = \frac{\alpha}{1-\alpha} \cdot I_B + \frac{1}{1-\alpha} \cdot I_{CBO}}$

(3) characteristics of CB connection

→ The relationships between voltages and currents of a transistor can be displayed and the curve obtained are known as the characteristics of transistor.

→ Two main characteristics are —

(1) Input characteristics —



→ It is the curve between emitter current I_E and emitter-base voltage V_{EB} at constant collector-base voltage V_{CB}.

→ Here I_E is taken along y-axis & V_{EB} is taken along x-axis.

→ From the graph it is clear that the I_E increases rapidly with small increase in V_{EB}. So, i/p resistance is very small.

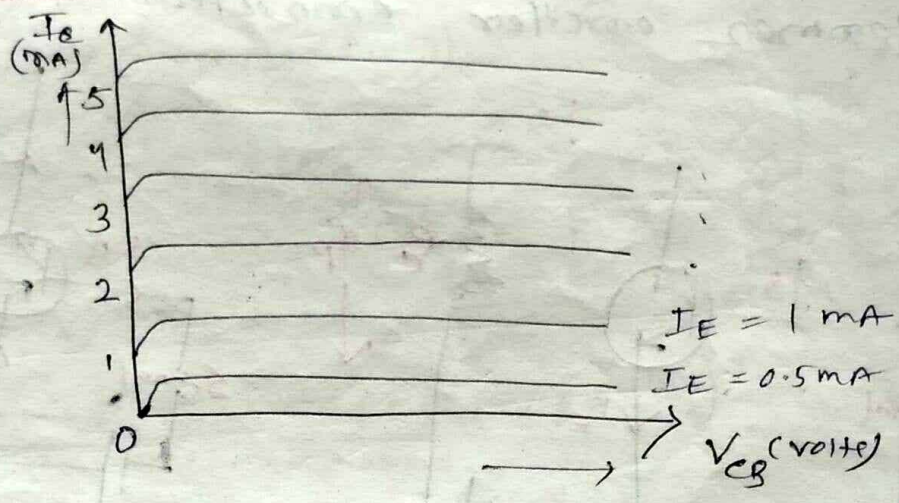
→ The I_E and I_c are independent to collector voltage V_{CB}.

Input resistance :- (r_i)

→ It is the ratio of change in emitter-base voltage (ΔV_{EB}) to the change in emitter current (ΔI_E) at constant V_{CB} i.e.

$$r_i = \frac{\Delta V_{EB}}{\Delta I_E}, \text{ at constant } V_{CB}$$

(2) **Output characteristics :-**



→ It is the curve between collector current I_C and collector-base voltage V_{CB} at constant emitter current I_E.

→ Here collector current is taken along y-axis's V_{CB} along x-axis.

→ From the graph it is clear that I_C varies with V_{CB} only at small voltages (<1V) and above 1-2 V, the I_C remains constant indicated by straight horizontal curve.

Output resistance :- (r_o)

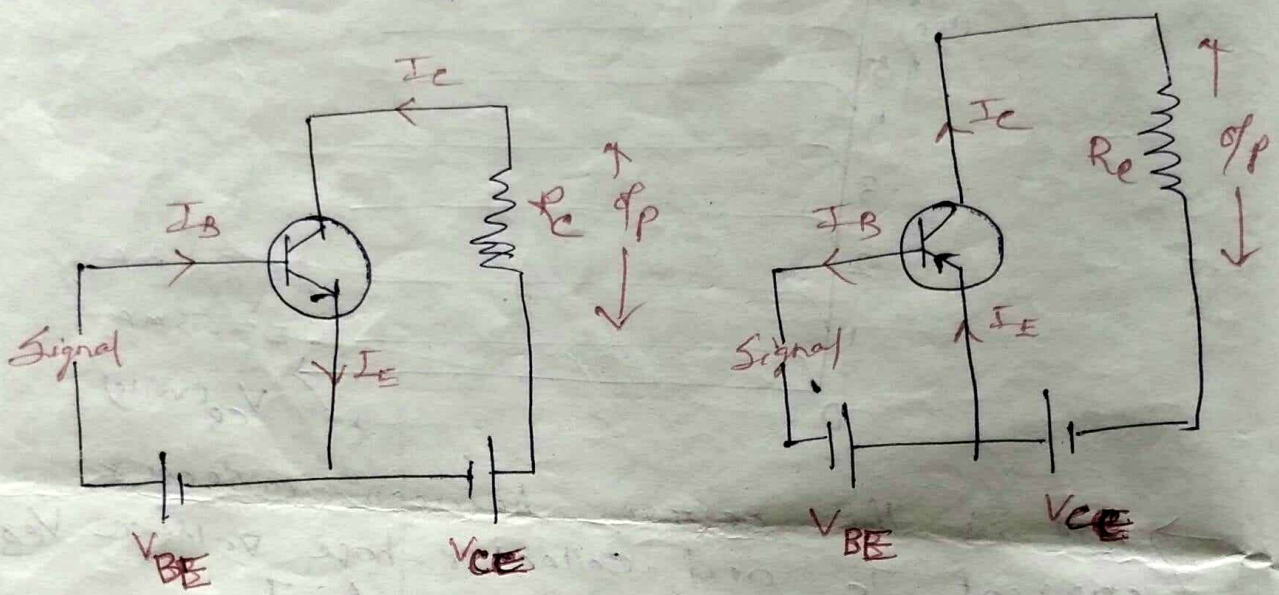
→ It is the ratio of change in collector-base voltage (ΔV_{CB}) to the change in collector current (ΔI_C) at constant I_E i.e.

$$r_o = \frac{\Delta V_{CB}}{\Delta I_C}, \text{ at contant } I_E$$

(ii) Common emitter Connection :—

→ In this connection, i/p is applied between base and emitter and o/p is taken from collector and emitter.

→ Hence, emitter is common to both i/p and o/p circuits & hence the name common emitter connection.



(1) Base current amplification factor (β) :—

→ The ratio of change in collector current (ΔI_C) to the change in base current (ΔI_B) is known as base current amplification factor i.e.

$$\beta = \frac{\Delta I_C}{\Delta I_B}$$

→ Usually, β value ranges from 20 to 500.

(2) Expression for collector current :—

→ In CE connection, I_B is the i/p current and I_C is the o/p current.

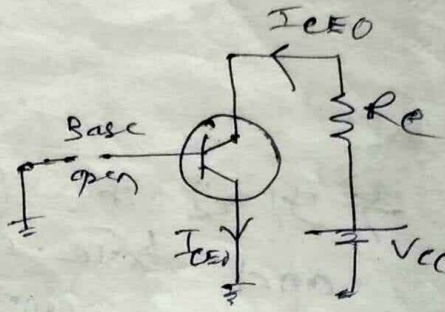
We know, $I_E = I_B + I_C$

$$I_C = \alpha I_E + I_{CBO}$$

$$\Rightarrow I_C = \alpha(I_B + I_C) + I_{CBO}$$

$$\Rightarrow I_C = \frac{\alpha}{1-\alpha} \cdot I_B + \frac{I_{CBO}}{1-\alpha}$$

If base (i/p) is open i.e. $I_B = 0$ then the collector current flows is known as collector cut off current which is small in value but much larger than I_{CBO} (in CB-connection).



So, $I_C = \frac{1}{1-\alpha} \cdot I_{CBO}$ $(\because I_B = 0)$

Now, $I_C = \frac{\alpha}{1-\alpha} \cdot I_B + I_{CEO}$

$$\Rightarrow \boxed{I_C = \beta \cdot I_B + I_{CEO}} \quad (\because \beta = \frac{\alpha}{1-\alpha})$$

Relation between β and α :-

We know, $\alpha = \frac{\Delta I_C}{\Delta I_E}$ ——— (i)

$\beta = \frac{\Delta I_C}{\Delta I_B}$ ——— (ii)

Now, $I_E = I_B + I_C$

$\Rightarrow \Delta I_E = \Delta I_B + \Delta I_C$

$\Rightarrow \Delta I_B = \Delta I_E - \Delta I_C$

Substituting ΔI_B in eq (ii), we get

$$\beta = \frac{\Delta I_C}{\Delta I_E - \Delta I_C}$$

Dividing the numerator and denominator of R.H.S by ΔI_E, we get,

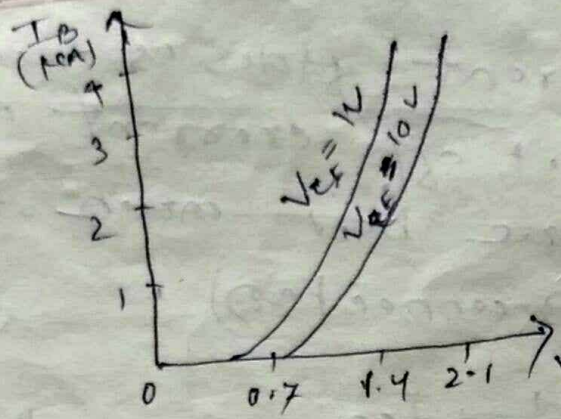
$$\beta = \frac{\Delta I_C / \Delta I_E}{\frac{\Delta I_E}{\Delta I_E} - \frac{\Delta I_C}{\Delta I_E}} = \frac{\alpha}{1-\alpha} \quad (\because \alpha = \frac{\Delta I_C}{\Delta I_E})$$

$$\Rightarrow \boxed{\beta = \frac{\alpha}{1-\alpha}}$$

(3) characteristics of CE connection:

→ Two main chars. :—

(1) Input characteristics :—



→ It is the curve between base current I_B and base-emitter voltage V_{BE} at constant collector-emitter voltage V_{CE}.

→ Here I_B is along y-axis and V_{BE} along x-axis.

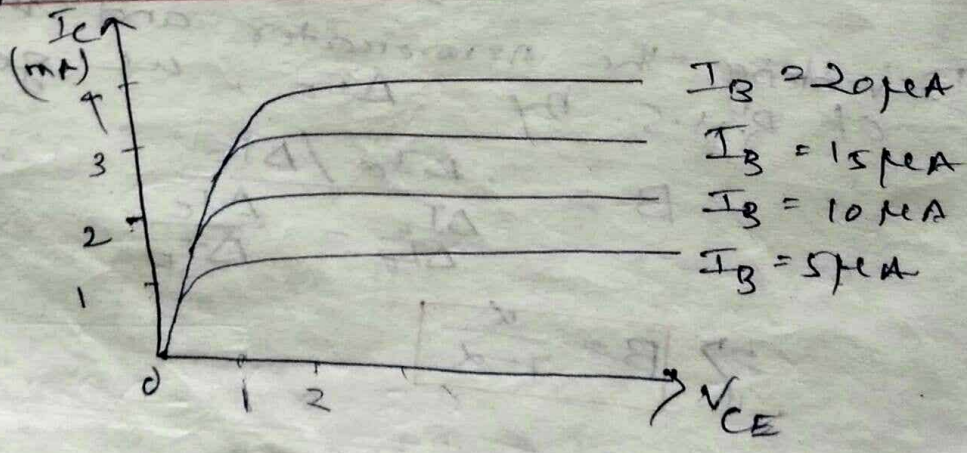
→ In I_B increases less rapidly with V_{BE}.

Input resistance :— (r_i)

It is the ratio of change in base-emitter volt. (ΔV_{BE}) to change in ΔI_B at constant V_{CE} i.e.

$$r_i = \frac{\Delta V_{BE}}{\Delta I_B}, \text{ at constant } V_{CE}$$

(2) Output characteristics :—



→ It is the curve between collector current I_C and collector-emitter voltage V_{CE} at constant I_B.

→ Here I_C along y-axis & V_{CE} along x-axis.

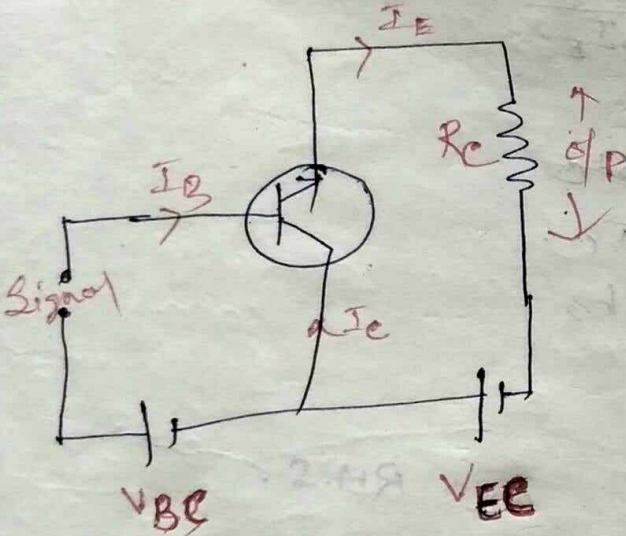
→ From the graph it is clear that I_C varies with V_{CE} between 0 and 1V only. After this, I_C becomes almost constant.

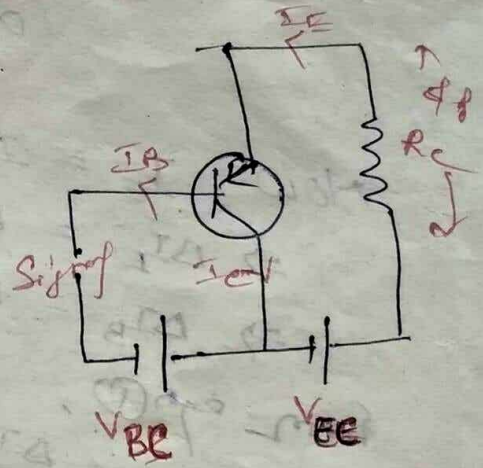
Output resistance :- (r_o)

→ It is the ratio of change in collector-emitter voltage (ΔV_{CE}) to the change in collector current (ΔI_C) at constant I_B

i.e. $$r_o = \frac{\Delta V_{CE}}{\Delta I_C}, \text{ at constant } I_B$$

(iii) Common Collector Connected :-





→ In this circuit arrangement, i/p is applied between base and collector while o/p is taken between the emitter and collector.

(1) Current amplification factor (γ) :-

→ The rated of change in emitter current (ΔI_E) to the change in base current (ΔI_B) is known as current amplification factor (γ).

i.e. $\boxed{\gamma = \frac{\Delta I_E}{\Delta I_B}}$

(2) Expression for collector current :-

We know, $I_C = \alpha I_E + I_{CBO}$

$I_E = I_B + I_C$

$\Rightarrow I_E = I_B + (\alpha I_E + I_{CBO})$

$\therefore I_E(1-\alpha) = I_B + I_{CBO}$

$\Rightarrow I_E = \frac{I_B}{1-\alpha} + \frac{I_{CBO}}{1-\alpha}$

or $\boxed{I_C \simeq I_E = (\beta+1) I_B + (\beta+1) I_{CBO}}$

$\left(\because \beta = \frac{\alpha}{1-\alpha} \right.$

$\left. \Rightarrow \beta + 1 = \frac{\alpha}{1-\alpha} + 1 = \frac{1}{1-\alpha} \right)$

Relation between γ & α

We know, $\gamma = \frac{\Delta I_E}{\Delta I_B}$ ——— (I)

$\alpha = \frac{\Delta I_C}{\Delta I_E}$ ——— (II)

Now, $I_E = I_B + I_C$

$\Rightarrow \Delta I_E = \Delta I_B + \Delta I_C$

$\Rightarrow \Delta I_B = \Delta I_E - \Delta I_C$.

from eqn (I), we get,

$\gamma = \frac{\Delta I_E}{\Delta I_E - \Delta I_C}$

Now, dividing ΔI_E on R.H.S.

$\gamma = \frac{\Delta I_E / \Delta I_E}{\frac{\Delta I_E}{\Delta I_E} - \frac{\Delta I_C}{\Delta I_E}} = \frac{1}{1-\alpha}$

$\left(\because \alpha = \frac{\Delta I_C}{\Delta I_E} \right)$

$\Rightarrow \boxed{\gamma = \frac{1}{1-\alpha}}$

Relation between γ & β :-

$\boxed{\gamma = \beta + 1}$ $\gamma = \frac{\Delta I_E}{\Delta I_B} = \frac{\Delta I_B + \Delta I_C}{\Delta I_B}$ (Divide by ΔI_B)

$\Rightarrow \gamma = \frac{1+\beta}{1} \Rightarrow \boxed{\gamma = \beta + 1}$

Transistor Load line Analysis :—

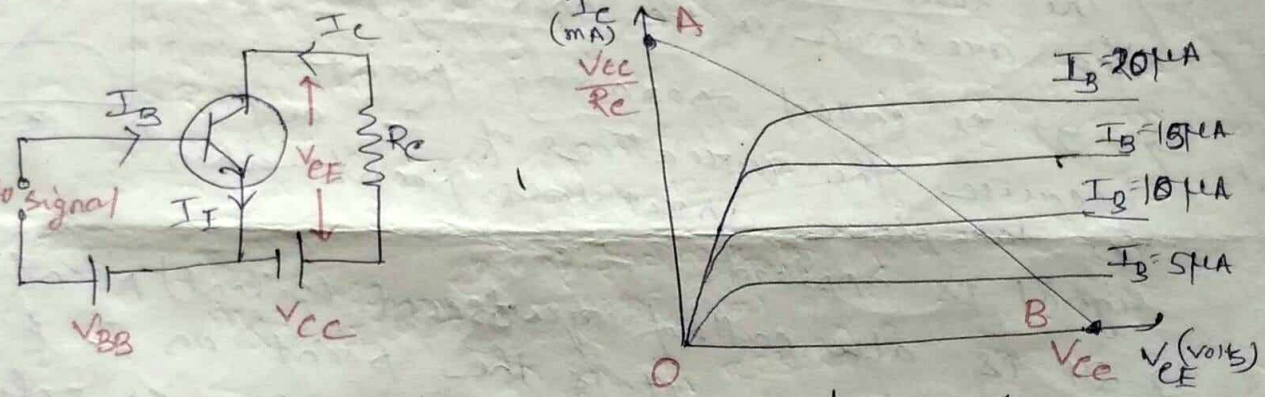
→ Load line method is used to determine the collector current for various collector-emitter voltages through the load.

→ This method is frequently used in the analysis of transistor applications.

d.c. Load line :-

→ It is the line on the output characteristics of a transistor ckt which gives the value of I_c and V_{CE} corresponding to zero signal or d.c. conditions.

→ Consider a CE npn transistor ckt,



→ The o/p characteristics is shown here.

→ The value of collector-emitter voltage V_{CE} at any time is given by,

$$V_{cc} - I_c R_c - V_{CE} = 0$$

$$\Rightarrow \boxed{V_{CE} = V_{cc} - I_c R_c}$$

→ As V_{cc} and R_c are fixed values, therefore it is a 1st degree equation and can be represented by a straight line on the o/p characteristics. this is known as d.c. loadline.

→ 1st we need two points of the straight line

(i) When $I_c = 0$, then collector-emitter volt. is maximum i.e. $V_{CE} = V_{cc} - I_c R_c$

$= V_{cc} - 0 \quad (\because I_c = 0)$

$$\Rightarrow \boxed{V_{CE} = V_{cc}}$$

This gives the 1st point B $(OB = V_{cc})$.

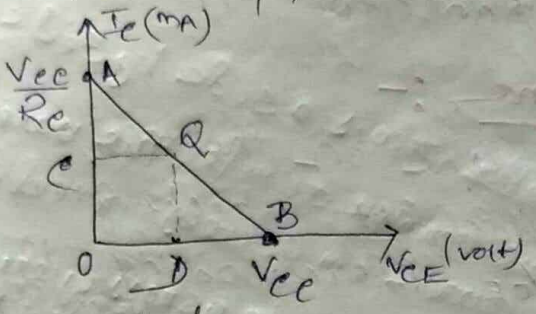
(ii) when $V_{CE} = 0$, then collector current is maximum,

$$V_{CE} = V_{cc} - I_c R_c$$

$$\Rightarrow 0 = V_{cc} - I_c R_c$$

$$\Rightarrow \boxed{I_c = V_{cc}/R_c}$$

This gives the 2nd point A ($OA = V_{cc}/R_c$).

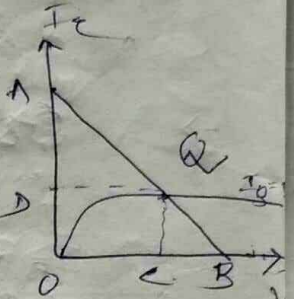


Operating point :-

→ The zero signal values of I_c and V_{CE} are known as the operating point.

→ It is called operating point because the variations of I_c and V_{CE} take place about this point when signal is applied.

→ It is also called quiescent (silent) point or Q-point because it is the point on I_c & V_{CE} characteristics when the transistor is silent i.e. in the absence of the signal.

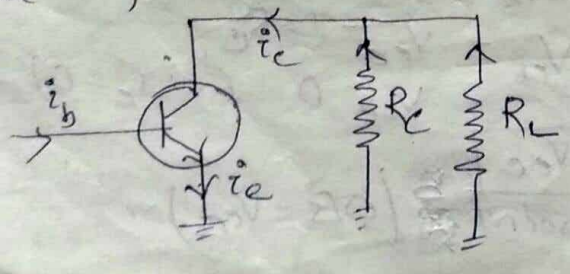


→ Suppose in the absence of signal, the base current is 5 μA & the o/p characteristic with loadline AB is shown in the figure.

→ The Q-point is obtained where the load-line & the characteristic curve intersects.

a.c. Load line :-

→ This is the line on the output characteristics of a transistor ckt which gives the values of i_c and V_{CE} when signal is applied.



→ Again we require two end points, one maximum collector-emitter voltage point (V_{CE}) & the other is maximum collector current point (I_c)

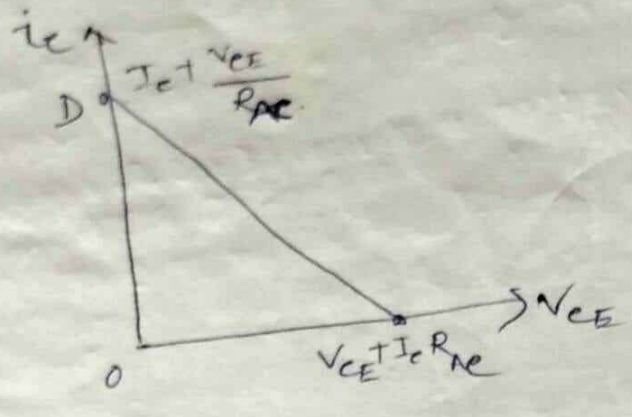
→ when a.c. signal is applied.

Max. i_c due to a.c. signal $= I_c + \frac{V_{CE}}{R_{AC}}$

∴ Max. collector emitter volt.

$= V_{CE} + I_c R_{AC}$

where $R_{AC} = \frac{R_c R_L}{R_c + R_L}$ i.e. $R_c \| R_L$



Transistor Biasing :-

→ The process of raising the strength of a weak signal without any change in its general shape is known as faithful amplification.

→ For faithful amplification, a transistor amplifier must satisfy three conditions -

(i) Proper zero signal collector current.
(ii) Proper base-emitter voltage at any instant
(iii) Proper collector-emitter voltage at any instant.

def → The proper flow of zero signal collector-current and the maintenance of proper collector-emitter voltage during the passage of signal is known as transistor biasing.

→ The basic purpose of biasing is to keep the BE junction properly forward biased and CB junction properly reverse biased during the application of signal.

→ This is achieved by a bias battery or a circuit with a transistor.

Stabilisation :-

→ The I_C in a transistor depends on -
(i) the temperature changes.
(ii) Variations of transistor parameters.

def → The process of making operating point independent of temperature changes or variation in transistor parameters is known as stabilisation.

→ So, stabilisation is needed for I_C due to. -

(i) Temperature dependence of I_C :-

(eqn) $I_C = \beta I_B + I_{CEO}$ (for CE ckt)

→ A rise of 10°C doubles the collector leakage current which may rise to 0.2mA for Ge transistor.

(ii) Individual Variations :- The value of β & V_{BE} are not same for any two transistors even of same type.

(iii) Thermal runaway :-

The I_C for CE configuration is

$$I_C = \beta I_B + (\beta+1) I_{CBO} = \beta I_B + \beta I_{CEO} \quad \text{---(1)}$$

→ The flow of I_C produces heat within the transistor.

→ If no stabilisation is done, the rise in temp. increases the collector leakage current, I_{CBO}.

→ Again, increase in $(\beta+1) I_{CBO}$ increases I_C.

→ This effect is cumulative and I_C becomes very large which causes the transistor to burn out.

→ So, the self-destruction of an unstabilised transistor is known as thermal runaway.

→ To avoid this, it is essential that the operating point is stabilised i.e. I_C is kept constant.

Stability Factor :-

→ The rate of change of collector current I_C w.r.t. the collector leakage current I_{CO} (I_{CBO} in CB) at constant β and I_B is called stability factor i.e.

$$S = \frac{dI_C}{dI_{CO}} \text{ at const. } I_B \text{ \& } \beta$$

→ For thermal stability, stability factor should be as low as possible.

→ For CE configuration —

$$I_C = \beta I_B + (\beta+1) I_{CO}$$

Differentiating w.r.t I_c we get,

$$\Rightarrow 1 = \beta \frac{dI_B}{dI_c} + (\beta+1)\frac{dI_{co}}{dI_c}$$

$$\Rightarrow 1 = \beta \frac{dI_B}{dI_c} + \frac{(\beta+1)}{S} \qquad \left[\because \frac{dI_{co}}{dI_c} = \frac{1}{S}\right]$$

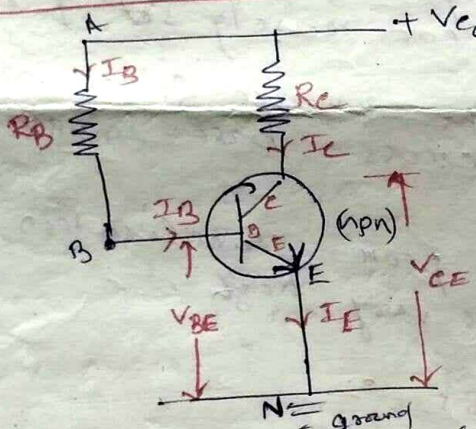
$$\Rightarrow \boxed{S = \frac{\beta+1}{1-\beta\left(\frac{dI_B}{dI_c}\right)}}$$

Methods of Transistor Biasing :-

→ Four methods are there :—

(i) Base resistor method / Fixed Biasing
(ii) Emitter bias method.
(iii) Biasing with collector-feedback resistor
(iv) Voltage-divider bias or potential-divider method.

Base Resistor Method :-



→ A high resistance R_B (several hundred kΩ) is connected between the base & +ve end of supply for npn tr. & for pnp tr it is base & -ve end.

Let I_c be the zero signal collector current.

$$\therefore I_B = \frac{I_c}{\beta}$$

→ Consider the closed ext ABENA & applying Kirchhoff's voltage law (KVL),

$$V_{cc} - I_B R_B - V_{BE} = 0$$

$$\Rightarrow V_{cc} = I_B R_B + V_{BE}$$

$$\Rightarrow I_B R_B = V_{cc} - V_{BE}$$

$$\Rightarrow \boxed{R_B = \frac{V_{cc} - V_{BE}}{I_B}}$$

As $V_{CC} \gg V_{BE}$,

$$R_B = \frac{V_{CC}}{I_B} \quad \text{and} \quad I_C = \beta I_B$$

- Now, Applying KVL at o/p side,

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$\Rightarrow V_{CE} = V_{CC} - I_C R_C$$

Stability factor :—

We know, $S = \frac{\beta + 1}{1 - \beta\left(\frac{dI_B}{dI_C}\right)}$

- Here, I_B is dependent of I_C, so, $dI_B/dI_C = 0$

$$S = \beta + 1$$

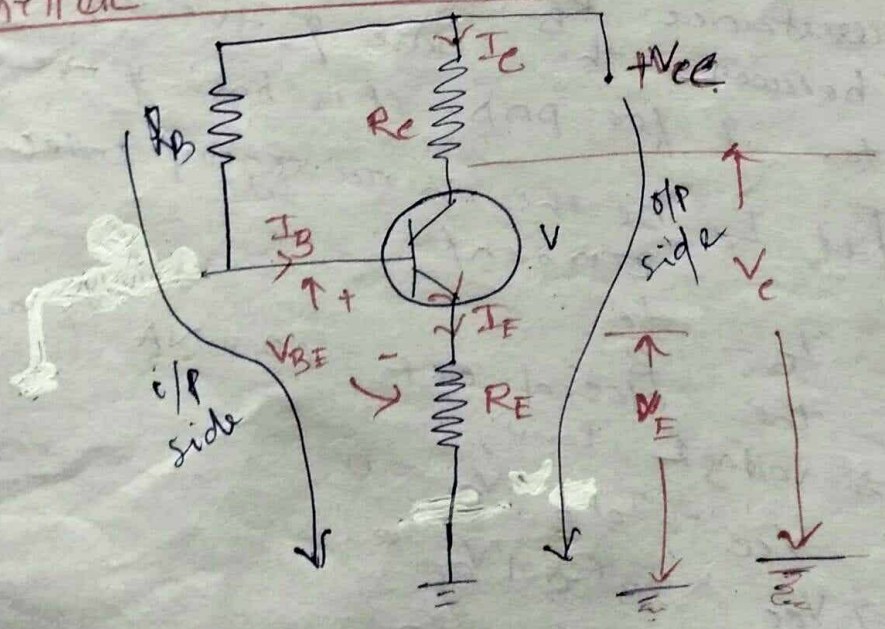
Advantages :—

(i) Biasing ckt is very simple.
(ii) Biasing conditions can easily set & calculations are simple.
(iii) No loading of the source since no resistor is employed across base-emitter junction.

Disadvantages :—

(i) This method provides poor stabilisation.
(ii) Stability factor is very high.

Emitter Bias Circuit :—



→ Here, an Emitter resistant (R_E) is present across the emitter terminal as shown in the figure.

→ A supply voltage V_{cc} ; R_C, R_B are also present.

Now, Apply KVL to i/p side,

$$V_{cc} - I_B R_B - V_{BE} - I_E R_E = 0 \quad \text{—(1)}$$

Here $I_c \approx I_E$ & $I_c = \beta I_B$ i.e. $I_E = \beta I_B$.

From eq^n,

$$V_{CC} - I_B R_B - V_{BE} - \beta I_B R_E = 0$$

$$\Rightarrow V_{cc} - I_B(R_B + \beta R_E) - V_{BE} = 0$$

$$\Rightarrow I_B(R_B + \beta R_E) = V_{cc} - V_{BE}$$

$$\Rightarrow \boxed{I_B = \frac{V_{cc} - V_{BE}}{R_B + \beta R_E}}$$

& $\boxed{I_c = \beta I_B}$ ⟹ collector Current

Apply KVL to o/p side,

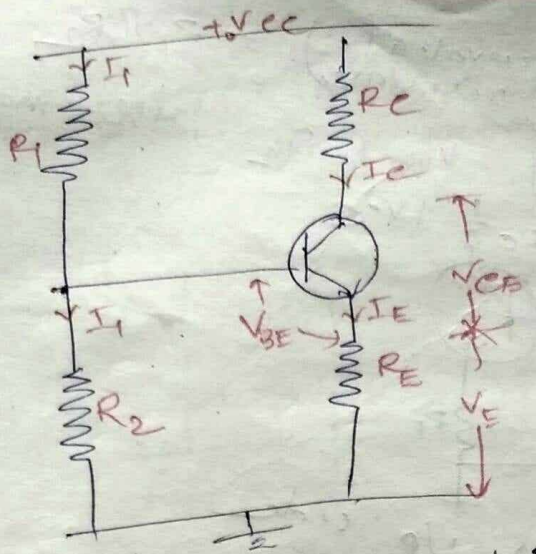
$$V_{CC} - I_c R_C - V_{CE} - I_E R_E = 0$$

$$\Rightarrow V_{cc} - I_c R_c - V_{CE} - I_c R_E = 0$$

$$\Rightarrow \boxed{V_{CE} = V_{cc} - I_c(R_c + R_E)}$$

↳ Collector–Emitter Voltage.

Voltage Devider Bias method:-

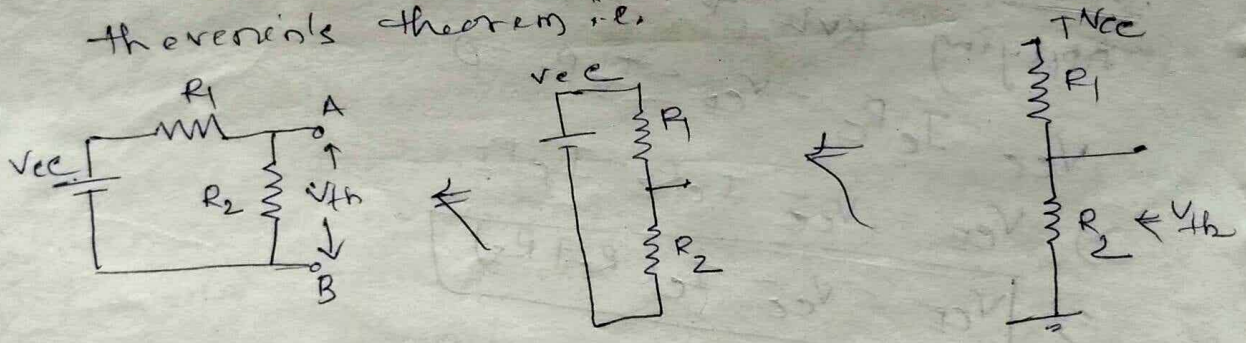


→ In this method R_1 and R_2 resistors are connected from Vcc to ground in such a way that the total voltage is devided into two parts from which the lower part is applicable for biasing.

→ R_E is used for stabilization.

collector current (I_C)

Now, the i/p section is modified by thevenin's theorem i.e.



V_{th} = thevenin voltage = the potential across R_2 (lower resistance)

I_1 = current through R_2 = $\frac{Vcc}{R_1+R_2}$

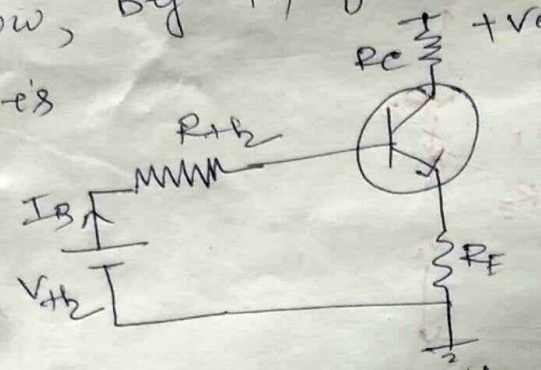
$\therefore V_{th} = \left(\frac{Vcc}{R_1+R_2}\right) \cdot R_2$

Apply KVL to ~~Base ckt~~

→ From the ckt diagram,

R_{th} (Equivalent resistance) $= R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2}$

Now, by applying V_{th} & R_{th}, the modified ckt is



Applying KVL to i/p side

$V_{th} - I_B R_{th} - V_{BE} - I_E R_E = 0$

$\Rightarrow V_{th} - I_B R_{th} - V_{BE} - (\beta+1) I_B R_E = 0$

$\Rightarrow \boxed{I_B = \frac{V_{th} - V_{BE}}{R_{th} + (\beta+1) R_E}}$

& $\boxed{I_c = \beta I_B}$

VCE:

Applying KVL to o/p side.

$V_{cc} - I_c R_c - V_{CE} - I_E R_E = 0$

$\Rightarrow V_{CE} = V_{cc} - I_c R_c - I_c R_E$

$\Rightarrow \boxed{V_{CE} = V_{cc} - I_c (R_c + R_E)}$

Now $V_{CE} = V_C - V_E$

$\Rightarrow \boxed{V_c = V_{CE} + V_E}$

$V_{BE} = V_B + V_E$

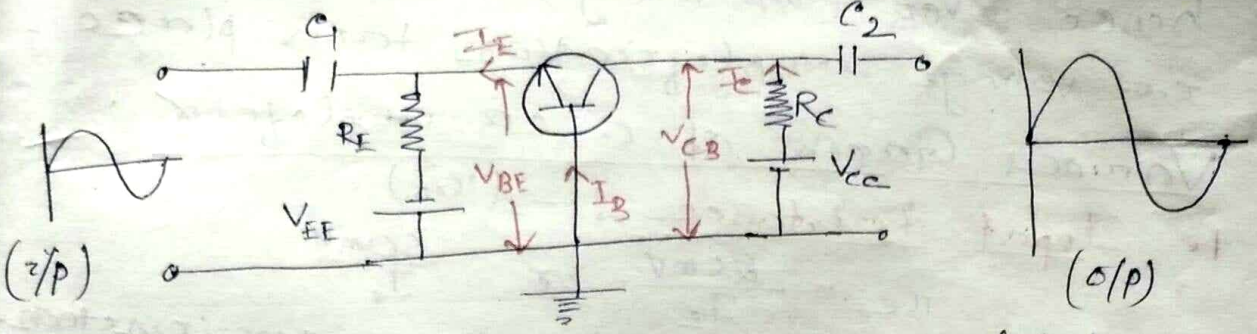
$\Rightarrow \boxed{V_B = V_{BE} + V_E}$

& $\boxed{V_E = I_E R_E}$

Stability factor: $S = (\beta+1) \frac{1}{1+\beta+1} = ($

AMPLIFIERS :-

Common Base (CB) Amplifier :-



→ This figure shows the CB amplifier using NPN transistor.

→ The EIB junction is forward biased by V_{EE} and CIB junction is reverse biased by V_{cc}.

→ When no signal is applied to the i/p circuit (CKT), the o/p is at Q-point so that there is no o/p signal.

→ When an ac signal is applied to EIB junction via a coupling capacitor C_1 then following operation takes place.

circuit operation :-

1) Forward biased is decreased as V_{BE} is when positive half cycle is applied than -ve w.r.t. ground.

2) Consequently, I_B is decreased.

3) I_E and hence I_C is decreased.

4) Drop $I_C R_C$ is decreased.

5) Hence, V_{CB} is increased as per the equation $V_{CB} = V_{cc} - I_C R_C$.

→ This means a positive o/p half-cycle is produced.

→ In this ckt i/p resistance is less as forward biased & o/p resistance is

high as reverse biased.

→ So, according to the ckt operation ac drop across load is very large & hence V_{CB} (o/p voltage) is much larger i.e. voltage amplification takes place.

Various Gains of a CB amplifier :—

1. Input Resistance :— (r_{in})

$$r_e = \frac{25mV}{I_E} \text{ or } \frac{50mV}{I_E}$$

this is the resistance in emitter junction

∴ I/p resistance, $\boxed{r_{in} = r_e // R_E}$

2. Output Resistance :— (r_o)

$\boxed{r_o = R_c}$

If a load resistance R_L is connected then

$\boxed{r_o = R_c // R_L}$

3. Current Gain :— (A_i)

$\boxed{A_i = \alpha}$ α = current amplification factor.

4. Voltage Gain :— (A_v)

$$\boxed{A_v = \frac{r_o}{r_{in}} = \frac{r_o}{r_e}}$$

5. Power Gain : (A_p)

$\boxed{A_p = A_v \cdot A_i}$

In decibel, $\boxed{G_p = 10 \log_{10} A_p \text{ dB}}$

characteristics of CB :—

1) Very low i/p resistance (30 - 150Ω)
2) Very high o/p resistance (upto 500K).
3) Current gain $\alpha < 1$
4) Large voltage gain of about 1500.
5) Power gain of upto 30 dB.
6) Phase relation ship between i/p and o/p

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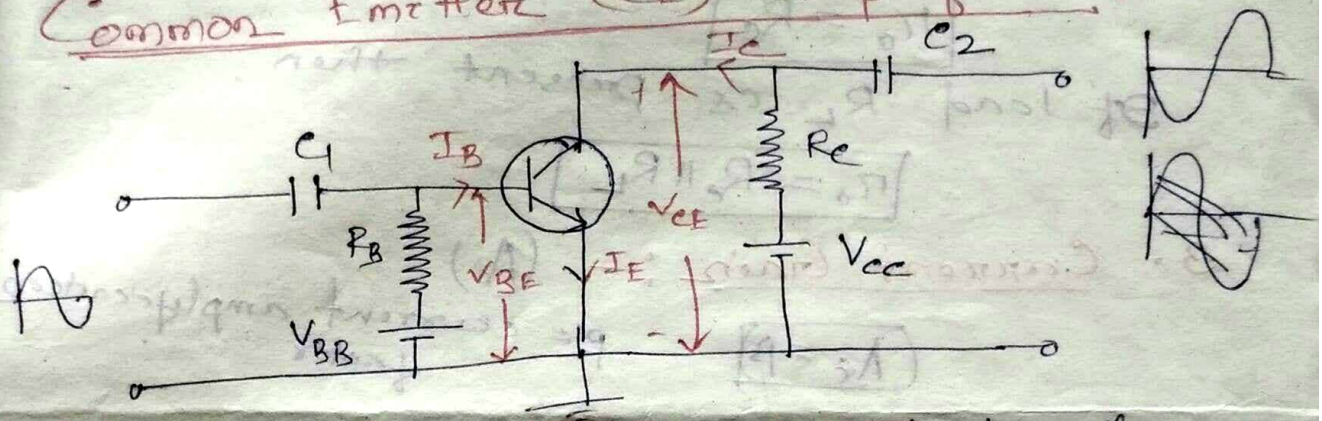
→ Since, a positive-going i/p signal produces a positive-going o/p signal there is no phase reversal between the i/p and o/p voltages.

Uses :-

→ In matching a low-impedance ckt to a high impedance ckt.

→ It has high stability of I_C with temp. changes.

Common Emitter (CE) Amplifier :-



→ Here, i/p signal is injected into the B/E ckt and o/p is taken from C/E junction of a NPN transistor.

→ The dc equation is -

$$I_B \cong V_{BB}/R_B$$

$$I_C = \beta I_B \quad \&$$

$$\boxed{V_{CE} = V_{CC} - I_C R_C}$$

Circuit Operation :-

When +ve half cycle is applied,

1) V_{BE} is already increased because it is +ve w.r.t the ground.

2) It leads to increase in forward bias of B/E junction.

3) I_B is increased.

4) So, I_C is increased as $\beta = \frac{I_C}{I_B}$.

5) Drop $I_C R_C$ is increased.

6) V_{CE} is decreased as seen from the eqn.

Various Gains of a CE amplifier :-

1. **Input Resistance :-** (r_{in})

When viewed from base, ac resistance of emitter junction is βr_e.

So, i/p resistance $r_{in} = R_B \parallel \beta r_e \simeq \beta r_e$

2. **Output Resistance :-** (r_o)

$$r_o = R_c$$

If load R_L is present then,

$$r_o = R_c \parallel R_L$$

3. **Current Gain :-** (A_i)

$A_i = \beta$ $\quad$ β = current amplification factor.

4. **Voltage Gain :-** (A_v)

$$A_v = \beta \cdot \frac{r_o}{r_{in}} = \beta \cdot \frac{r_o}{\beta \cdot r_e} \simeq \frac{r_o}{r_e}$$

5. **Power Gain :-** (A_p)

$$A_p = A_v A_i = \beta \cdot \frac{r_o}{r_e}$$

or $G_p = 10 \log_{10} A_p$ dB

Characteristics of CE amplifier :

1) It has moderately low i/p resistance (1k to 2k)
2) It's o/p resistance is moderately large (50 k or so).
3) It's current gain (β) is high.
4) It has very high voltage gain of order of 1500 or so.

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5) It produces very high power gain of the order 10,000 times or 40dB.

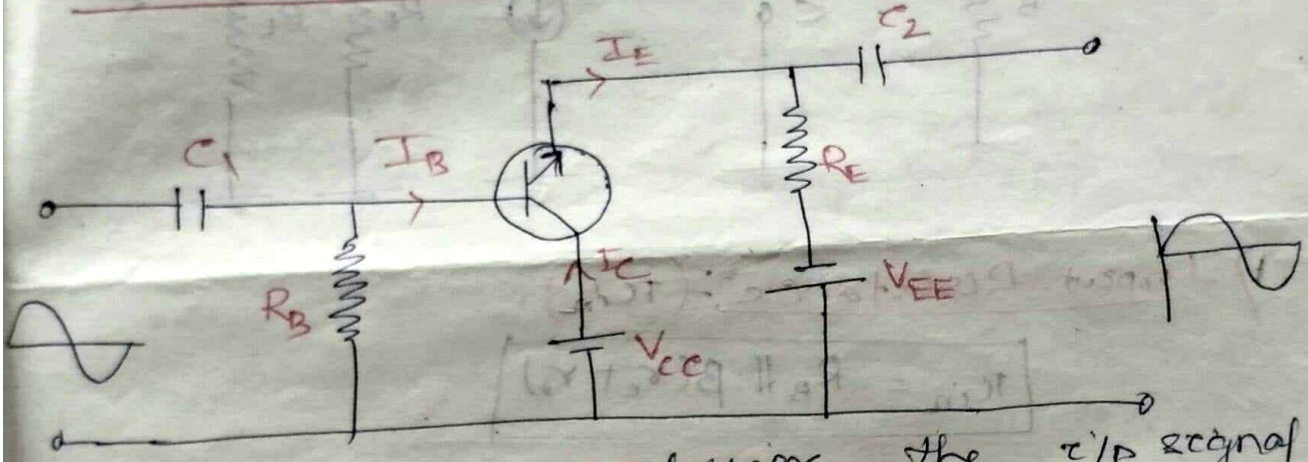
6) phase relationship :—

→ It produces phase reversal of i/p signal i.e. i/p and o/p signals are 180° out of phase with each other.

Uses :—

→ Most transistor amplifiers are CE type because of large gain in voltage, power & current.

Common Collector (cc) amplifier :—



→ In the cc amplifier, the i/p signal is applied across B/C junction & o/p signal is taken out from E/C junction.

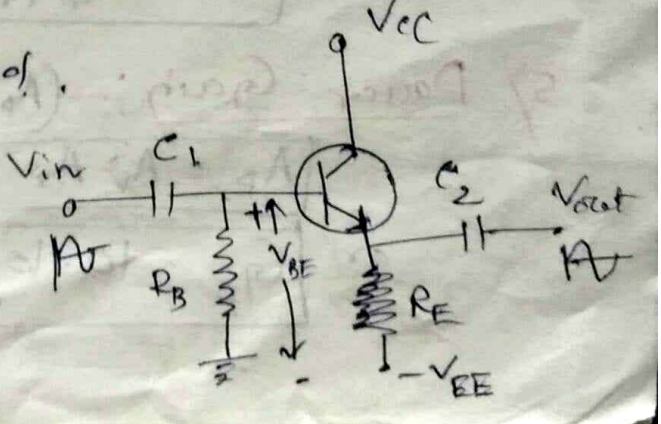
→ Again E/B is forward biased by V_{EE} & C/B is reverse biased by V_{CC}.

→ Here, $$I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta} \cong \frac{V_{EE}}{R_E + R_B/\beta}$$

Circuit Operation :—

When +ve half is applied.

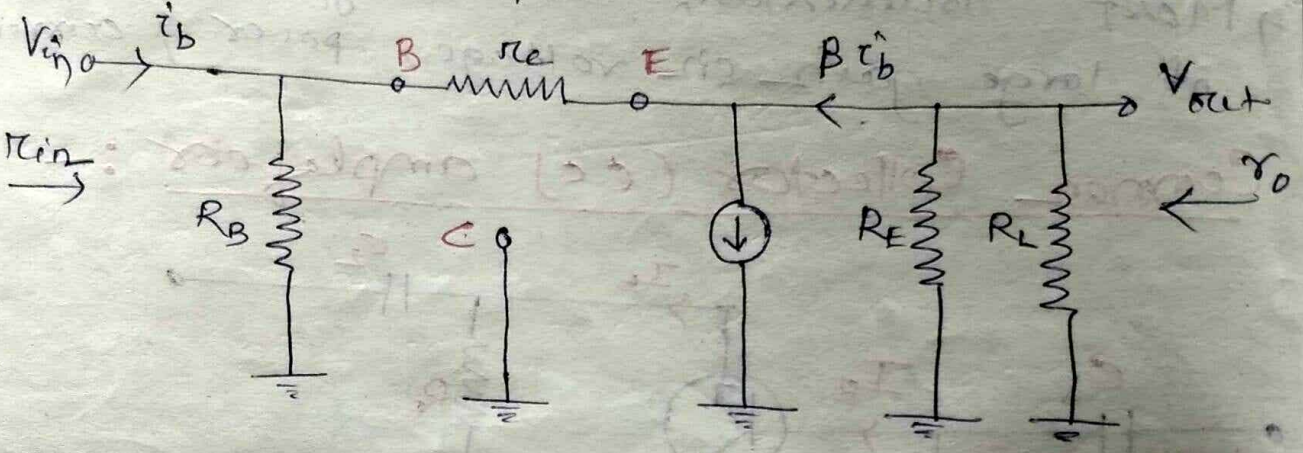
1) Forward biased is increased as V_{BE} is +ve w.r.t. collector i.e. ground.



2) I_B is increased.
3) I_E is increased.
4) Drop across R_E is increased i.e. $I_E R_E$
5) hence, o/p volt. (drop across R_E) is increased

Various Gains of a cc amplifier :—

The a.c. equivalent ckt. of cc ampl



1) Input Resistance :- (r_{in})

$$r_{in} = R_B \parallel \beta(r_e + r_o)$$

2) Output Resistance :— (r_o)

$$r_o = R_E \parallel R_L$$

3) Current Gain :— (A_i)

$$A_i = \beta$$

4) Voltage Gain :— (A_v)

$$A_v = \frac{r_o}{r_o + r_e}$$

Usually $r_o \gg r_e$

$$A_v \cong \frac{r_o}{r_o} = 1.$$

5) Power Gain :—(A_p)

$$A_p = A_v A_i$$

or

$$G_p = 10 \cdot \log_{10} A_p \text{ dB}$$

Characteristics of cc amplifier :-

1) It has high i/p impedance (20-500 kΩ).
2) It has low o/p impedance (50-150 Ω).
3) High current gain (1+β) i.e. (50-300).
4) Voltage gain of less than 1.
5) Power gain of 10 to 20dB.
6) Phase relationship :-

→ No phase reversal between i/p and o/p signals.

Uses :-

→ For impedance matching i.e. for connecting a circuit having high o/p impedance to one having low i/p impedance.
→ For circuit isolation.
→ As a two-way amplifier since it can pass a signal in either direction.
→ For switching circuits.

Amplifier classification Based on Biasing condition :-

→ This classification is based on the amount of transistor bias and amplitude of the i/p signal i.e. ~~It~~ ~~takes~~ the portion of the i/p cycle for which the transistor conducts.

→ Types :-

(a) class-A amplifier :-

→ In this case, the transistor is so biased that o/p current flows for the full cycle of the i/p signal (360°) i.e. transistor remains forward biased throughout the i/p cycle.

→ Hence, the conduction angle is 360°.

(b) class-B Amplifier :-

→ In this case, the tr. bias and the amplitude of i/p signal are such that o/p current flows for half-cycle (180°) of the i/p cycle.

→ It means tr. stays forward biased for half the i/p cycle.

→ The tr. conduction angle is 180°.

(c) class-C Amplifier :-

→ In this case, tr. bias and signal amplitude are such that o/p current flows for less than half cycle of the i/p signal i.e. 120° or 150° angle of conduction.

→ In other words, tr. remains forward biased for less than half the cycle.

(d) class-AB Amplifier :-

→ The characteristics of such an amplifier lie in-between those of class-A and class-B.

→ Here, o/p current flows more than half but less than the entire cycle i.e. current flows for more than 180° but less than 360°.